Temperature Distribution in Multichip IGBT Module and Its Impact on Collector Current Sharing

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Abstract: Multichip Insulated Gate Bipolar Transistor (IGBT) power modules are widely used in high power applications. However, the parallel connection of IGBT chips results in an inhomogeneous temperature/current distribution. In this paper, a thermographic camera is used to capture the temperature distribution of an opened Infineon IGBT module FF600R17ME4 where each IGBT switch has three IGBT chips. The influence of temperature distribution on collector current sharing is then examined in both healthy conditions and bond wire lift-off scenarios. In this research, the critical temperature distribution is demonstrated experimentally at both chip and switch levels. The experimental results reveal that there are, depending on the collector current, 8°C to 60°C temperature difference at the chip level and 2°C to 10°C maximum temperature variation at the switch level. The severe temperature distribution impacts the collector current sharing less than 1% variation under healthy conditions and 0.507% at \( I_c = 240 \text{ A} \) upon the first bond wire lift-off. Other findings are that during homogeneous temperature distribution current densities are nearly similar per chip and less dependent on chip temperatures. Findings of this research have the potential to influence multichip Insulated Gate Bipolar Transistor (mIGBT) layout design. For example, having investigated the current density distribution at different operating points, it is recommended to increase the number of bond wires by 11% for the chip placed in the middle for this particular module in order to increase reliability. Potential future research areas have also been identified.

Keywords: Multichip Insulated Gate Bipolar Transistor; Temperature Distribution; Collector Current Sharing

1. Introduction

Nowadays, several Insulated Gate Bipolar Transistor (IGBT) chips are paralleled to increase the current ratings of the IGBT module. The parallel connection of IGBT chips, however, also induces problems, such as inhomogeneous temperature/current distribution which are two primary aging indicators in IGBT modules [1]. Few studies have been published on temperature variations between chips in multichip Insulated Gate Bipolar Transistor (mIGBT) modules. For instance, in [2] and [3], the temperature variations measured between chips are about 5°C and 15°C, respectively. About 10°C variations are captured across the chip surface by [4]. Temperature is a critical indicator for the reliability of power electronics [5, 6]. For every 10°C increment in average temperature, the failure rate nearly doubles [7]. From these studies, it can be noted that the temperature difference between different chips is remarkable and therefore should not be ignored. Consequently, it is of paramount importance to scrutinize the Inhomogeneous Temperature distribution (ITD) in a mIGBT and investigate its impacts.

In recent years, the impacts of ITD on virtual junction temperature \( T_{VJ} \) estimation is vastly explored. Sundaramoorthy [8, 9] created a lateral temperature difference between two chips in an IGBT module with a heater and fan cooler. Then, double pulse tests were conducted to capture the Miller plateau width \( t_{Miller} \) for \( T_{VJ} \) estimation. In [8, 9], the baseplate temperature was measured to represent the temperature of the IGBT chips which is not an accurate representation of the chip temperature. Temperature Sensitive Electrical Parameters (TSEPs), \( V_{CE(on−load)} \) was studied under ITD condition in [10]. The ITD condition was generated by a current pulse train injected into the IGBT module. With the help of an infrared (IR) camera (SC5500/SC7500 MWBB), significant temperature divergence within one chip was captured at the end of the current pulse. The
ITD condition leads to a notable $T_{vj}$ estimation error of $V_{CE(on-load)}$. The authors in [7] studied the impact of ITD on two TSEPs, internal gate resistor $R_G(int-chip)$ and on-state voltage under sense current $V_{CE(on-sense)}$, for $T_{vj}$ estimation. Here, the ITD condition is created between two IGBT chips, with one chip kept at 100°C and $T_{vj}$ of the other chip varying from 60°C to 140°C. It has been found that the temperature predicted by $R_G(int-chip)$ is close to $T_{vj}$, whereas the temperature predicted by $V_{CE(on-sense)}$ is slightly higher than $T_{vj}$. The authors in [11] investigated the impact of temperature distribution on ten representative TSEPs. Results showed that $V_{CE(on-sense)}$ is the most accurate TSEP for Homogeneous Temperature distribution (HTD) and ITD conditions. However, in ITD conditions, temperatures predicated by $V_{CE(on-load)}$, $dV_{CE}/dt$, and $V_{CE(peak)}$ are lower than actual $T_{vj}$, and temperatures predicated by $I_C(tail)$ and $g_m$ are lower than $T_{vj}$. The work in [7-11] provides an insight about the impact of ITD on $T_{vj}$ estimation in mIGBTs. Authors in [12, 13] also investigated the temperature distribution (TD) between IGBT chips, comprehensive experiments have been carried out to investigate the temperature evolution and evaluation when the mIGBT is subjected to bond wire lift-offs. The results show that 1) the degradation of one die leads to the redistribution of the current towards healthy dies which tends to equilibrate the lifetime of the different dies in the presence of an initial imbalance, 2) $V_{CE(on-sense)}$ underestimates the $T_{oj}$ as degradation propagates.

Although the temperature distribution (TD) between semiconductor chips is known, surprisingly there is a lack of exhaustive description of TD in both chip level and switch level. Furthermore, the impact of TD on collector current $I_c$ distribution has not been studied experimentally. The collector current $I_c$ flowing through the IGBT module generates power loss which causes expansion mismatch of different materials in the module and finally leads to faster aging of the IGBT devices. This situation can be improved by the optimization of packaging and layout, for instance, the number of bonding points in a chip.

This paper studies the temperature distribution in mIGBT modules and its impact on Collector current $I_c$ distribution. The investigation is carried out by analyzing the data captured from the thermographic camera. The findings of this work could be utilized to guide the packaging and layout design of mIGBT modules.

The paper is organized as follows: In Section 2, comprehensive experiments are carried out to depict the TD in mIGBTs. TD in both chip level and switch level is presented and analyzed. The impact of TD on collector current sharing is studied in Section 3. In this study, $I_c$ distribution under both healthy conditions and bond wire lift-off conditions is considered. Further discussion is carried out in Section 4. In the discussion, an example is provided to illustrate how to apply the results to optimize the bonding points in a chip. Finally, the conclusion is summarized in Section 5.

2. Investigation of temperature distribution on FF600R17ME4

To inspect the TD within an mIGBT, power cycling experiments are conducted on FF600R17ME4. TD is examined at both chip level and switch level, which provides the exhaustive TD assessment.

2.1 Power cycling test setup

The FF600R17ME4 IGBT is a 1200 V/600 A, a half-bridge module from Infineon with three IGBT chips for each switch, as shown in Figure 1. The chips in one switch are highlighted with boxes. These three chips are referred to as Chip1, Chip2, and Chip3. The maximum collector current density is 166.6A/cm². To capture the TD with the IR camera, the IGBT switch is coated with black matt paint to increase the emissivity of the chip surface. After coating, the emissivity is about 0.95 [14]. Then, the IGBT module is mounted on a water-cooling plate controlled by a chiller (Liquid Cooler WAR7042N07ZTP0 7035). The temperature of the chiller is set to 20°C. However, in the experiment, the temperature will fluctuate between 17°C to 22°C due to the control system of the chiller.

![Figure 1. The layout of the FF600R17ME4 IGBT Module [11]. The sliver part inside the yellow box indicates the surface of the IGBT chip. Bond wire: Chip1 has 11, Chip2 has 13, Chip3 has 13. Bonding points: Chip1 has 44, Chip2 has 29, Chip3 has 29.](image-url)
Figure 2(a) shows the schematic of the test rig. The full set-up is shown in Figure 2(b) [11]. During operation, the IGBT is in on-state with +15V on the Gate-Emitter (G-E) terminal. Then, a current pulse is injected into the IGBT through the Collector-Emitter (C-E) terminals by the TopCon DC power supply. An IR camera monitors the temperature distribution of the IGBT chips during the test. Table I lists the injected current during the experiment and the ratio of the injected current to the rated current of the power module.

Table 1: Load conditions of the IGBT module under test.

<table>
<thead>
<tr>
<th>Test current</th>
<th>180A</th>
<th>300A</th>
<th>420A</th>
<th>540A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ratio to rated current / %</td>
<td>30</td>
<td>50</td>
<td>70</td>
<td>90</td>
</tr>
</tbody>
</table>

2.2 TD assessment

Power cycling tests are carried out to assess the TD of the IGBT switch. The injected current pulse and the corresponding thermal distribution of the IGBT switch are shown in Figure 3. As shown in Figure 3(a), it takes a few milliseconds for the power supply to raise the current level to the set value; this phase is known as the rising phase. Once the current reaches the demand value, the current is held for a few seconds to allow the accumulation of thermal distribution; this phase is known as the holding phase. Different holding times are used to magnify the thermal impact caused by the power loss. In both phases, $T_{vj}$ of the IGBT module will increase over time. After the pulse current is switched off, $T_{vj}$ decreases. Figure 3(b) corresponds to the thermography of the IGBT switch when the injected current is 300 A and $t_{pulse} = 12$ s. The triangle at the center indicates the hottest spot within the scope of the camera, whereas the triangle at the edge shows the coldest point. The temperature of the chip is higher than that of the bond wires and the temperature of Chip2 is the highest.

The IR images captured in each test condition are used to quantify the temperature distribution. The virtual junction temperature of the IGBT chip $T_{vj}$ is the average temperature within the surface area as shown in Figure 3 (b). And the corresponding global virtual junction temperature $T^*_{vj}$ of the miIGBT switch was derived with equation (1).
\[ T_{vj} = \left[ T_{vj,1}S_1 + T_{vj,2}S_2 + T_{vj,3}S_3 \right] / (S_1 + S_2 + S_3) \]

where \( i \) is the chip number and \( S_i \) is the surface area of the \( i \)-th chip. \( T_{vj,i} \) is the virtual junction temperature of the \( i \)-th chip.

Furthermore, for the IR image shown in Figure 3 (b), there is a maximum, average, and minimum temperature within each IGBT chip. Therefore, the temperature fluctuation can be further divided into \( \Delta T_{(\text{max})} \), \( \Delta T_{(\text{avg})} \) and \( \Delta T_{(\text{min})} \) as expressed in Equation (2), (3), and (4).

\[ \Delta T_{(\text{max})} = T_{(\text{max})@t2} - T_{(\text{max})@t0} \]
\[ \Delta T_{(\text{avg})} = T_{(\text{avg})@t2} - T_{(\text{avg})@t0} \]
\[ \Delta T_{(\text{min})} = T_{(\text{min})@t2} - T_{(\text{min})@t0} \]

Figure 4 displays the average temperature fluctuation \( \Delta T_{(\text{avg})} \) for each IGBT chip during the power cycling test. \( t_{\text{pulse}} \) varies from 1 s to 15 s. The test at \( I_C = 420 \) A is halted at \( t_{\text{pulse}} = 7s \) while the test at \( I_C = 540 \) A is halted at \( t_{\text{pulse}} = 2s \). This is to ensure that \( T_{vj} \) of the IGBT switch does not exceed the safe operation boundary. In this case, the safe operation boundary means the maximum temperature the IGBT chip could stand without self-damage. Figure 4 depicts that \( \Delta T_{(\text{avg})} \) of each chip climbs with the rise of the current level \( I_C \) as well as \( t_{\text{pulse}} \). The temperature will eventually level out if \( t_{\text{pulse}} \) is long enough. The temperature increment varies slightly from chip to chip. Due to the package layout, the chip in the middle (Chip2) is always the hottest, whereas Chip3 is the coldest.

2.2.1 TD within each chip

TD within each chip is evaluated through the maximum temperature difference \( \Delta T_{C_i(\text{max})} - \Delta T_{C_i(\text{min})} \). \( C_i \) refers to Chip \( i \). Results for all three chips are depicted in Figure 5 as a function of \( I_C \) and \( t_{\text{pulse}} \). Figure 5 shows that the temperature difference between the hottest and the coldest points is small at \( I_C =180 \) A. However, a dramatic increase in temperature variance is observed for all three chips at \( I_C = 300 \) A, which is 50% of the rated current. The maximum temperature difference in Chip2 \( \Delta T_{C2(\text{max})} - \Delta T_{C2(\text{min})} \) reaches about 60°C at \( I_C = 540 \) A. Overall, the maximum temperature difference \( \Delta T_{C(i\text{(max)})} - \Delta T_{C(i\text{(min)})} \) of each chip varies between 8°C and 60°C. Consequently, the TD within each chip is significant. This will lead to inhomogeneous thermal stress for the IGBT chip, which will cause non-uniform thermal expansion within the silicon IGBT chip layers.
temperature differences among the IGBT chips and also higher they are different from Chip3. 

2.2.2 TD within the IGBT switch 

TD within the IGBT switch is evaluated via the maximum disparity of the temperature fluctuation among the three IGBT chips. Therefore, corresponding to \( \Delta T_{Ci(max)} \), \( \Delta T_{Ci(avg)} \) and \( \Delta T_{Ci(min)} \), the maximum disparities within the IGBT switch are classified into \( T_{S(max)} \), \( T_{S(avg)} \) and \( T_{S(min)} \). The definitions of the disparity are expressed in Equation (5), (6), (7).

\[
T_{S(max)} = \max(\Delta T_{C1(max)}, \Delta T_{C2(max)}, \Delta T_{C3(max)}) - \min(\Delta T_{C1(max)}, \Delta T_{C2(max)}, \Delta T_{C3(max)})
\]

\[
T_{S(avg)} = \max(\Delta T_{C1(avg)}, \Delta T_{C2(avg)}, \Delta T_{C3(avg)}) - \min(\Delta T_{C1(avg)}, \Delta T_{C2(avg)}, \Delta T_{C3(avg)})
\]

\[
T_{S(min)} = \max(\Delta T_{C1(min)}, \Delta T_{C2(min)}, \Delta T_{C3(min)}) - \min(\Delta T_{C1(min)}, \Delta T_{C2(min)}, \Delta T_{C3(min)})
\]

The maximum disparity among the three IGBT chips is illustrated in Figure 6. In general, the \( T_{S(max)} \), \( T_{S(avg)} \) and \( T_{S(min)} \) are between 2°C to 16°C and rise with \( I_C \) and \( t_{pulse} \). The \( T_{S(max)} \) of the IGBT switch is 2°C - 10°C, which is about 2°C lower than \( T_{S(avg)} \). The highest disparity is observed in \( T_{S(min)} \), which is 2°C - 16°C. Unlike the other two, \( T_{S(min)} \) is almost the same at all current levels when the current pulse width is 1s. The reason is that the minimum temperature tends to designate the temperature of the bond wires. When the pulse width is 1s, the temperature increment upon different collector currents are similar to each other, thus the difference at four current levels is negligible.

3. Influence of ITD on Collector current \( I_C \) distribution 

In this section, the influence of ITD on \( I_C \) distribution is studied under both healthy conditions and bond wire lift-off conditions.

3.1. Healthy condition 

The double pulse test setup has been used to carry out the tests under healthy conditions. The temperature distribution in Figure 3(b) was emulated by using externally controlled hot and cooling plates as shown in Figure 7(a) [11]. In the setup shown in Figure 7(a), the cooling plate is connected to a liquid chiller and the temperature is kept constant at 15°C. The temperature of the heat plate is regulated via (Weller WHP300) and can, therefore, be varied. With this arrangement, the temperatures of Chip1 and Chip2 can be adjusted so that they are different from Chip3. In this setup, the increase of the cooling plate temperature will lead to larger temperature differences among the IGBT chips and also higher \( T_{ij} \) of the corresponding switch, and vice-versa.
The ITD test conditions are shown in Table 2. Three tests are carried out to imitate the similar condition as occur in practical application. Figure 7 (b) is an example of $I_C$ distribution at HTD condition. Noticeably, the current distribution is not uniform among the three IGBT chips. The current share in Chip2 is the largest and that of Chip3 is the smallest.

### Table 2. Temperature condition of three ITD tests.

<table>
<thead>
<tr>
<th>Test No.</th>
<th>$T_{j\text{-Chip1}}/\degree C$</th>
<th>$T_{j\text{-Chip2}}/\degree C$</th>
<th>$T_{j\text{-Chip3}}/\degree C$</th>
<th>$T_{vj}/\degree C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test 1</td>
<td>34.6</td>
<td>33</td>
<td>30.8</td>
<td>32.5</td>
</tr>
<tr>
<td>Test 2</td>
<td>45.7</td>
<td>44.0</td>
<td>40.4</td>
<td>43.5</td>
</tr>
<tr>
<td>Test 3</td>
<td>56.9</td>
<td>53.0</td>
<td>48.2</td>
<td>52.4</td>
</tr>
</tbody>
</table>

Figure 7. (a) Temperature control plate. (b) Example of collector current sharing. HTD test with $T_{vj} = 22.1\degree C$. (c) Thermography of the mIGBT under Test 3 (The cooling plate is set at 15 °C and the hot plate is set at 90 °C).

The current share of each chip is derived with Equation (8) and compared in Figure 8. The application of the percentage eliminates the influence of the current fluctuation, which is a common phenomenon between the turn-off transient of the first pulse and the turn-on transient of the second pulse in Figure 7.

$$ Percentage = \frac{I_C(\text{Chip})}{I_C} \times 100\% $$  \hspace{1cm} (8)

Figure 8. Collector current sharing (a) just before the first turn-off transient (b) after the second turn-on transient. Line plot: HTD test. Scatter plot: ITD test. The temperature axis represents the junction temperature $T_j$.

Figure 8 (a) and (b) depict the $I_C$ distribution in the IGBT switch just before the first turn-off transient and right after the second turn-on transient, respectively. In both figures, as long as the temperature distribution is uniform, the current distribution is constant and is not severely influenced by the temperature level. However, at ITD conditions, the current distribution changes. Despite the fact that the average temperature of the IGBT switch remains the same, the current share of the coldest chip, Chip3, is increasing, while the current share of Chip2 decreases. The IGBT chip in the module in Figure 1 is with a trench gate field stop structure. Since field stop IGBT does not use lifetime control and the mobility declines with temperature, the on-state voltage increases drastically which leads to a lower inflexion point [15]. This means the IGBT switch works in the positive temperature coefficient region in its forward characteristics. The coldest chip tends to share more current to
reduce the thermal stress of the hotter chip. This is the self-balancing principle so long as at least one chip is below the inflexion point.

3.2. Bond wire lift-off condition

The current sharing process upon bond wire failure is presented in Figure 9. Similarly, $I_C$ of each chip is presented which is the ratio of the chip currents $I_{C1}$, $I_{C2}$, and $I_{C3}$ to $I_C$ derived with Equation (8). It can be noted that the current share fluctuates with the temperature. However, it does not express any dependency on temperature. At the healthy state, the current share for Chip1, Chip2, and Chip3 are 32.5%, 38%, and 29.5%, respectively. As shown in Figure 9, when 4 out of 37 bond wires are lift off one by one in Chip1, the current share of Chip1 declines. On the contrary, the current share of Chip2 and Chip3 goes up. Figure 9 also shows that the variation of the percentages increases with the increment of the lifted bond wires. The trends shown is the same for all tests at $I_C = 40$ A, $I_C = 100$ A and $I_C = 240$ A. However, the deviation of the current share upon the first lift-off varies with the current level. For instance, the deviation upon the first lift-off at 40 A is 0.170%. This increases to 0.507% at 240 A. This indicates that the current redistribution becomes severe when the injected current is high.

Figure 9. Current distribution upon bond wire lift-off in Chip1 at $I_C = 240$ A.

4. Discussion

The main aging factors for an IGBT module are the silicon chip temperature variations, the maximal junction temperature, the case temperature swing, and the current density [1]. In this paper, the temperature distribution and its impact on collector current sharing are investigated in Section 2 and Section 3. The experimental results in section 2, reveal that at the chip level, the difference between the maximum and minimum temperature varies between 8°C and 60°C depending on the current level. While at the switch level, the largest difference between the maximum temperature of each chip varies from 2°C and 10°C. The severe temperature distribution impacts the collector current sharing as demonstrated in Section 3. The results show that, under healthy conditions, there is about 1% variation in the current distribution upon ITD conditions in the used power module. Under bond wire lift-off condition, the variation is 0.507% when $I_C = 240$ A. The current redistribution upon ITD conditions will lead to the current density increment of cooler chip or healthier chip. This phenomenon could lead to accelerated aging or critical failure if the chip current density or the maximum temperature of the chip exceeds a maximum allowable value.

Packaging of power modules are of paramount importance for the reliability of mIGBTs. On one hand, proper design minimizes asynchronous switching behavior of the gate among different chips. This alleviates the stress of individual IGBT chips. On the other hand, the package layout also influences the thermal loading of each IGBT chip. As it is known that mIGBTs consists of several types of materials with different coefficient of thermal expansion, differences in thermal loading leads to a mismatched lifespan for each chip. Knowing that reliability is determined by the weakest link, it is essential to identify that link. Proper package layout therefore improves reliability and ultimately the lifespan of the device.

The results in this paper have the potential to guide the layout design of mIGBTs and help to identify the root cause of aging mechanism, for instance, the identification of the location of critical weak spots with the help of methods in [16], the optimization of bonding points on the chip surface.

Take the FF600R17ME4 IGBT module in this research as an example, the number of bonding points in each IGBT chip is different from each other, Chip1 has more bonding points than Chip2 and Chip3. However, during
the operation, Chip2 always have the highest current share (4.7% more current than the average) and average/maximum temperature (about 10°C higher than the other two chips at $I_C = 420$ A, about 10% of the highest temperature). The bonding points influence the power dissipation and the resistance of the collector to the emitter path and consequently the current share. With this knowledge, it can be noted that the bonding points of Chip2 should be improved and that of Chip1 should be reduced. Assuming the bonding points of Chip1, Chip2 and Chip3 are $n_1$, $n_2$, and $n_3$, the resistance $R$ of each bond wire is the same. Considering the current share, $n_1$ should be $3R/((n_1 + n_2 + n_3))$. Also, by considering the thermal dissipation, and assuming the thermal resistance $R_0$ of each bonding point is the same, the number of bonding points of Chip2 should be increased by about 11.1%.

In general, mIGBT modules have anti-parallel diodes. The on-state characteristics of diodes are quite different from IGBTs. For a single diode, temperature increase will introduce more charging carriers and thus higher saturation current and lower forward voltage. In the inhomogeneous temperature distribution condition in mIGBTs, the anti-parallel diode with higher temperature will share more current than others, as there is more current flowing through it, the diode temperature will increase even more. Even though all the diodes share the same Direct-Copper-Bonding plate for heat dissipation, this could potentially lead to thermal run away in particular if they are operating close to the saturation condition. Therefore, as future work, the impact on temperature distribution caused by anti-parallel diodes should be investigated in more depth.

5. Conclusions

This paper investigates the temperature and collector current sharing of an opened Infineon IGBT module FF600R17ME4 which is a half-bridge module where each IGBT switch has three IGBT chips. The temperature distribution of this multichip IGBT power module is experimentally investigated at both chip and switch levels. The results show that the difference between the maximum and minimum temperature varies between 8°C and 60°C, indicating a remarkable inhomogeneous temperature distribution. Following this investigation, the impact of temperature distribution on collector current sharing was studied. This study is carried out in both healthy and aged conditions. As a result of the temperature distribution, collector current redistribution occurs reaching 1% deviation at 240 A. The results of this work may aid in the detection of critical weak spots in the power module as well as the optimization of layout which has been illustrated in the Discussion section. In the future, comprehensive layout design approach and the temperature distribution of diode shall be studied.

References


