A HIGH PRECISION AND LOW NOISE S/H CIRCUIT DESIGN FOR VIDEO SIGNAL SAMPLING

Xinquan Lai, Donglai Xu, Lvshun Hu and Hongyi Wang*

Institute of Electronic CAD, Xidian University, Xian, 710071, P. R. China
* School of Science and Technology, University of Teesside, Middlesbrough, TS1 3BA, UK

ABSTRACT

This paper presents an improved Sample/Hold (S/H) circuit design for analog LCD applications. The circuit possesses the dual characteristics of high sampling precision and low switch noise and is, thus, suitable for video signal sampling applications. In order to increase accuracy of sampling and to reduce switch noise, the design uses an operational amplifier with current-mode switch, which incorporates an improved buffer amplifier, and introduces a noise elimination technique by using differential amplifier. The simulation results show that for a typical signal sampling application and its Bi-CMOS implementation, the design has achieved a minimal signal distortion and significantly reduced noise effect.

1. INTRODUCTION

With the development of modern communication and multimedia systems, high performance display devices have been becoming increasingly important for video-based systems integration, particularly in wireless and portable applications. As one of the most basic components in analog display VLSI [1, 2], S/H circuit has been widely used in many LCD applications that require accurate and low-noise signal/data sampling, such as computer display terminals, video cameras, and 3G mobiles and so on. A typical S/H circuit consists of three major components: the operational amplifier OP, the S/H switch, and the buffer amplifier with high input impedance, as shown in Figure 1. When the switch SW is on, both the voltage across the holding capacitor C and the output voltage Vo vary with the input voltage Vs. When the switch SW is off, the voltage across the capacitor C remains constant and the output voltage Vo has the same value as that the Vs holds at the time of the SW being switched off. Thus, when switch signal consists of a series of periodical narrow pulses, the sampled signal, which is corresponding to the input voltage, can be obtained from output port. In this paper, an S/H circuit that is based on an operational amplifier with current-mode switch, an improved buffer amplifier and a noise elimination technique is presented. It features highly accurate signal sampling and significantly reduced switch noise for our intended applications.

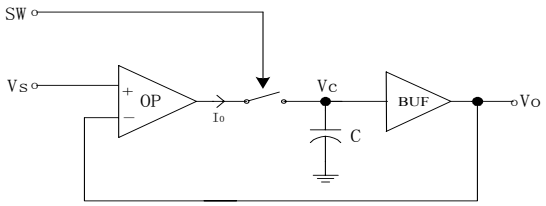

Figure 1. Diagram of a typical S/H circuit.

The rest of the paper is organised as follows. In section 2, an improved circuit design, focusing on sampling precision and switch noise, is described in detail. Section 3 presents the simulation results of the design and analyses performance. And finally, the conclusions are drawn in section 4.

2. IMPROVED CIRCUIT DESIGN

2.1 Improvement of Sampling Precision

Typically, JFET, NMOS, MOSFET, and transmission gate can be used as S/H switch. Although JFET and NMOS are structurally simple, this type of switch has a number of obvious drawbacks [3, 4]. When input voltage is high, resistance of the switch becomes significant while it is on. This leads to the result that the output signal Vo does not accurately trace the input signal Vs. This equivalent impedance of the switch also increases sampling time. For MOSFET switch, it has an inherent effect of channel charge injection, which reduces sampling precision. If a transmission gate is used as an S/H switch, it is difficult to ensure the simultaneous on/off operations of NMOS and PMOS, therefore resulting in unexpected sampling values and affecting sampling precision. In order to overcome these drawbacks and to improve sampling precision of S/H circuit, rather than using the switch structures discussed above, a new current-mode switch has been designed, as shown in Figure 2, which has the features of high bandwidth, high speed and high output impedance.

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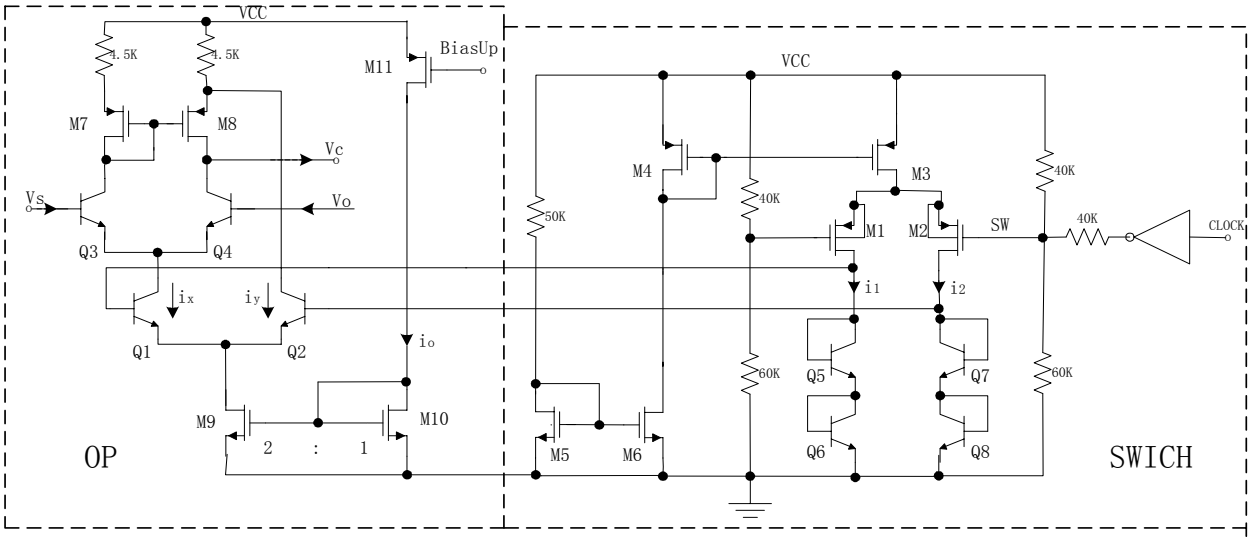

Figure 2. Schematic of the operational amplifier with current-mode switch.

In the circuit, a digital clock drives the transistors Q1 and Q2 through a current-mode comparator, and therefore controls the on/off operations of the operational amplifier OP. Here, i_o is bias current; i_1 and i_2 are the drain current of M1 and M2, respectively; i_x and i_y are the emitter current of Q1 and Q2, respectively. From the theory of the Trans-Linear-Loop [5], the following equations can be obtained.

$$i_x \cdot i_2^{\,2} = i_y \cdot i_1^{\,2} \ , \tag{1}$$

$$i_x + i_y = 2i_0 \ . \tag{2}$$

Thus, we have

$$i_x = 2i_0 \cdot \frac{i_1^2}{i_1^2 + i_2^2} \ , \tag{3}$$

$$i_y = 2i_0 \cdot \frac{i_2^2}{i_1^2 + i_2^2} \ . \tag{4}$$

When the digital clock signal is in the state of logic low, M1 is on in its saturation region and M2 is off. Thus, $i_1 >> I_2$, $i_x \approx 2i_o$, and $i_y \approx 0$. The sampling switch is effectively off. Otherwise, $i_x \approx 0$ and $i_y \approx 2i_0$; the sampling switch is effectively on. It is obvious that this structure improves switching performance in terms of sampling time, therefore improving sampling precision.

Due to restriction on the maximum operational frequency of the circuit, the holding capacitor C of the S/H circuit shown in the figure 1 has to have a modest value. This has implication on signal precision during holding time because input quiescent current becomes significant. To minimise the effect of the quiescent current on sampling precision, a buffer amplifier with high precision has been designed, as shown in Figure 3. In the circuit, output signal is obtained through Q9 and Q13. The constant current source formed by Q11 and Q12 keeps the emitter currents of Q9 and Q10 equal. During holding period, the base currents of Q9 and Q10 remain in the state of static balance, i.e., the base currents maintain their momentary values, which are present when the switch is being turned off. The two currents are supplied by the mirror current sources M12 and M13 and their values are equal. Therefore, the leakage current of the holding capacitor C is negligible and the variation of holding voltage is reduced to the minimum.

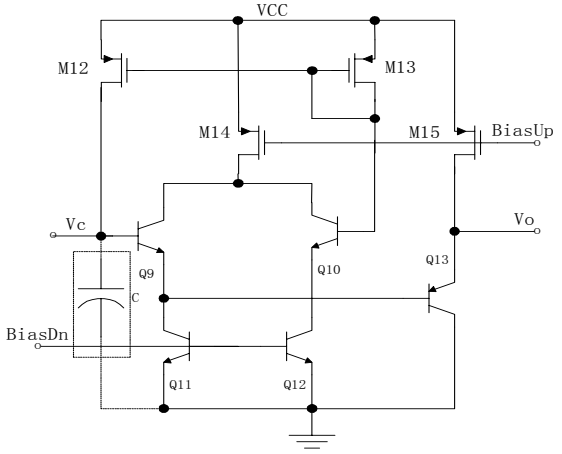

Figure 3. Buffer amplifier with high precision.

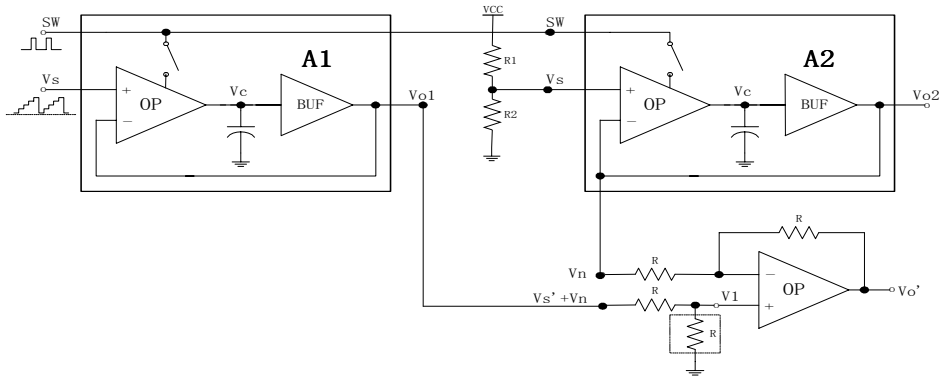

Figure 4. Diagram of noise elimination method.

2.2 Reduction of Switch Noise

In an S/H circuit, noise is mostly contributed by the switch noise, which is largely resulted from the fact that the transient response of clock pulse signal is added onto output through parasitic capacitor. This noise has great effect on the performance of the S/H circuit, particularly for video signal sampling applications [6]. In this section, a noise elimination method is introduced, as shown in Figure 4, to reduce the switch noise.

In the diagram, the module A1 and A2 are the S/H circuit with high precision described in the section 2.1. While the voltage value of resistors network is chosen to be the same as average level of video input signal, the output voltage V_{01} is equal to sum of sampling signal and noise voltage, and the output voltage V_{02} is static DC value with noise. Furthermore, since the noise voltages attracted by A1 and A2 are almost identical in terms of phase and amplitude, the AC outputs of A1 and A2 can be represented by V_S'+V_n and V_n (noise voltage), respectively. Thus, we have the following two equations

$$V_1 = \frac{V_S' + V_n}{2}, \tag{5}$$

$$V_0' = V_1 + \frac{V_1 - V_n}{R} R = V_S'. \tag{6}$$

Obviously, when the outputs of A1 and A2 are differentially filtered by a differential amplifier, the switch noise can be effectively eliminated.

3. SIMULATION RESULTS

To evaluate the performance of the designed circuit, the simulation has been carried out in HSPICE, which is based on a typical LCD video display application and a 0.8um Bi-CMOS process. Here, we assume that signal sampling frequency $f_{S/H}$ is given by [1]

$$f_{S/H} = \frac{N_{HP}}{T_{HS}}, \tag{7}$$

where N_{HP} is the number of pixels per row; T_{HS} is the time to scan all pixels in the row. If the LCD has a dot matrix of 881×228, sampling time is 55ns and holding time is 110ns (6.25MHz operation frequency), the relevant simulation results are shown in Figures 5 and 6, where sampling clock frequency is 6.25MHz and input signal is a sine wave with 1MHz frequency. The figure 5 suggests that after sampling, signal distortion has been relatively minor and signal integrity has been kept. The figure 6 shows the comparison between video signal sampling results with and without use of the noise elimination technique. It is evident that switch noise has been significantly reduced.

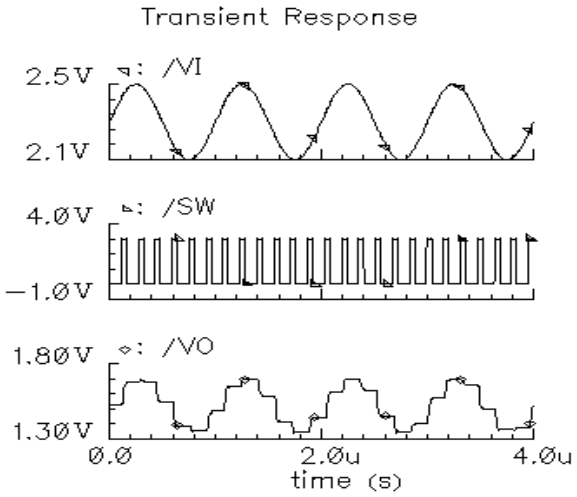

Figure 5. Result of sampling precision.

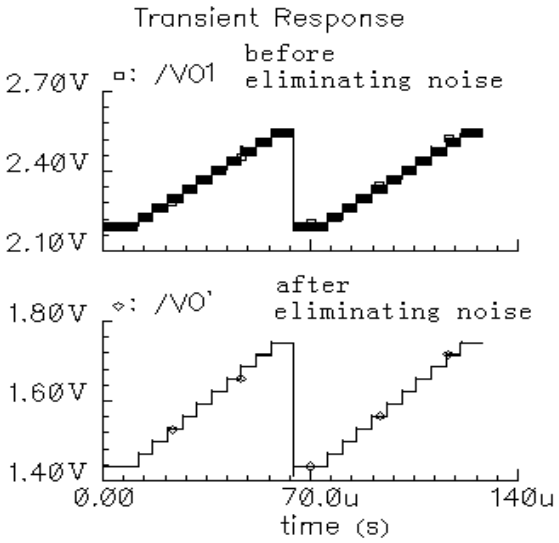

Figure 6. Result of noise elimination.

4. CONCLUSIONS

By introducing an operational amplifier with current-mode switch, a high precision buffer amplifier and a noise elimination method into the conventional S/H structures, a high precision and low noise S/H circuit has been designed for video signal sampling applications. The circuit analysis and simulation results show that the improved circuit design significantly increases sampling precision of S/H circuit and effectively reduces switch noise of the circuit.

5. REFERENCES

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