A Novel Reliability Estimation Methodology Towards the Design and Implementation of Symmetric Multilevel Inverter for Long Run Applications

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***Abstract*- Multilevel inverters are gaining attention in numerous applications due to their better performance attributes. Still, their utility in long-run applications remain as a critical concern due to the reliability issues. This work proposes a novel reliability estimation methodology tailored specifically for MLIs. The proposed reliability method employs advanced simulation techniques and statistical models to estimate the failure probabilities of critical components within the MLI. The proposed methodology provides more optimal assessment of the MLI's expected reliability over time. This enables designers and engineers to make informed decisions regarding component selection, system configuration, and maintenance schedules to enhance the long-term reliability of the MLI. Considering the drawbacks of the existing MLIs, this work has proposed a new symmetrical 7 level inverter with promising functional and reliability traits. The proposed topology appears to surpass existing topologies in several key metrics, including switching losses, reliability, THD, and component count. The performance of the proposed MLI have been validated through hardware results. These results show that the reliability methodology implemented can accurately estimate the MLI's reliability across various scenarios, enabling the identification of potential failure points and the formulation of strategies to mitigate reliability risks**.

I. INTRODUCTION

Power electronic research community in the past decades has shown more attention towards to the development, implementation, and application of multilevel inverter (MLI) topologies in various sectors such as renewable energy systems, general utility, electrical traction, and electric vehicles [1]-[7]. Multilevel inverters are capable to provide better quality output voltage with single or several DC voltage sources deployed in high and medium power conversion systems. The recent survey from the researchers clearly convey that the levels increment may lead to a greater number of power semiconductor devices procurement in MLI topology. The involvement of more switches will result in higher design complexity, more complementary conditions, and increased switching losses. Also due to higher number of switches the inverter suffers with lesser reduced lifetime and moderate reliability for the system [8]-[21]. Therefore, the real time implementation of the MLI is very critical. The design phase requirements and performance parameters to be taken care of during design process of the MLI are pictorially presented in Fig. 1.

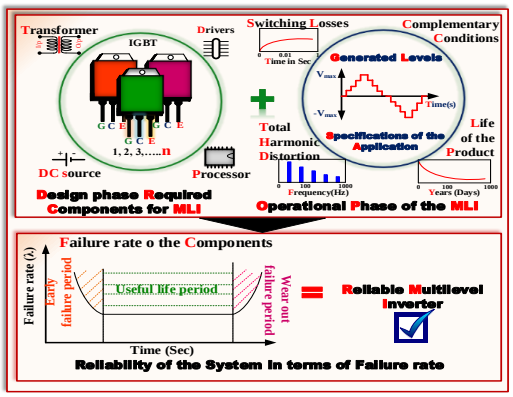

Fig. 1 Design phase requirements and performance parameters involved in the implementation of MLI.

Mainly the implementation of MLI is differentiated into symmetric and asymmetric multilevel inverters based on the DC source voltage involved in the topology. The voltage of each source must be equal in symmetric MLI but in asymmetric topologies the source voltage of each source will differ according to level generation. The asymmetric MLIs can generate a greater number of levels than the symmetric MLI with lesser number of switches but at the cost of higher implementation complexity. The selection of power semiconductor devices for asymmetric MLI is difficult because of the imbalanced operations due to the unequal voltage source combination and availability of different voltage sources also becomes a limitation. From operational point of view, the switching pattern involved with asymmetric MLI topologies incorporate higher complementary conditions and transitions due to more number of output levels with reduced part count. The two switches present in the same leg with inverted pulses to turn on the devices will normally result in short circuit issues with ideal pulse generation logic. This is referred as complementary condition. While the rising and falling instants in pulse generation which can make the switch

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turn on and off dynamics is referred as transitions condition. To implement in real time, the dead band generation is inevitable for safe operation of asymmetric topologies. The higher transitions in the power switches will lead to greater failure rate of individual devices [22]-[25]. The higher failure rate of the power switches will have an impact on the durability of the MLI. Also, it often calls for replacement of the power switches which is undesirable from successful product point of view. As a concluding remark, it can be stated that due to the fore mentioned limitations the symmetric MLI has been found to be a suitable topology. In the symmetric MLI, the compatibility of the switches can be easily reached along with lesser complementary conditions and transitions. This enhances the reliability of the symmetric topology as well. Because of these advantages, eight recent symmetric MLI topologies have been considered for investigation in this work. Also, from the listed drawbacks of the exiting topologies, a new symmetric MLI has been proposed and validated in this work.

The paper is organized as follows: The reliability evaluation methodology has been explained in Section II. Section III presents the review of existing MLI topologies with their limitations. Accounting all these drawbacks, a new MLI has been proposed in Section IV with required results. The functional and reliability attributes of all the topologies have been quantitatively detailed in Section V. To validate the new contribution, Section VI presents the hardware implementation of the proposed MLI. Finally, the paper is concluded in Section VII.

II. Proposed Reliability Evaluation Methodology

The constructional and operational attributes of the MLI are dependent on the quality facilities provided by the power switches. Usually, the performance of the power semiconductor device is defined with a life cycle as per the operation for specified application. According to that the operational life cycle of the power switches in MLI has been implemented for the long run applications. The operation characteristics of the power switch for a particular life cycle are called reliability. Mainly the reliability of power switches is dependent on the various factors at the level of constructional and operation called selection of the material, switch model, application for life cycle.

Based on the above statement the reliability evaluation process has been considered for the long-run applications of the MLI. Mainly the reliability methodologies have been formulated with the considerations of either historical or experimental data to find the failure rate of the electronic components. The historical data-oriented failure rate analysis can be implementable with the methodology of bottom-up-statistical (BS) method to select the proper components as per the simulation. The evaluation of fabricated hardware failure rate of the components can be estimated by using bottom-up-physics of failure (BP) methodology with necessary experimental data. Even though the hardware of MLI is designed with reliability measures, the components are suffering from more failure chances due to compatibility issues of components. Because in some cases the compatibility of BS method selected components are not compatible with real switches and BP method hardware fails to perform the operation to achieve the expected output as per the simulation. To facilitate optimal components selection during hardware implementation for reliable product development a novel evaluation process has been proposed as shown in Fig. 2.

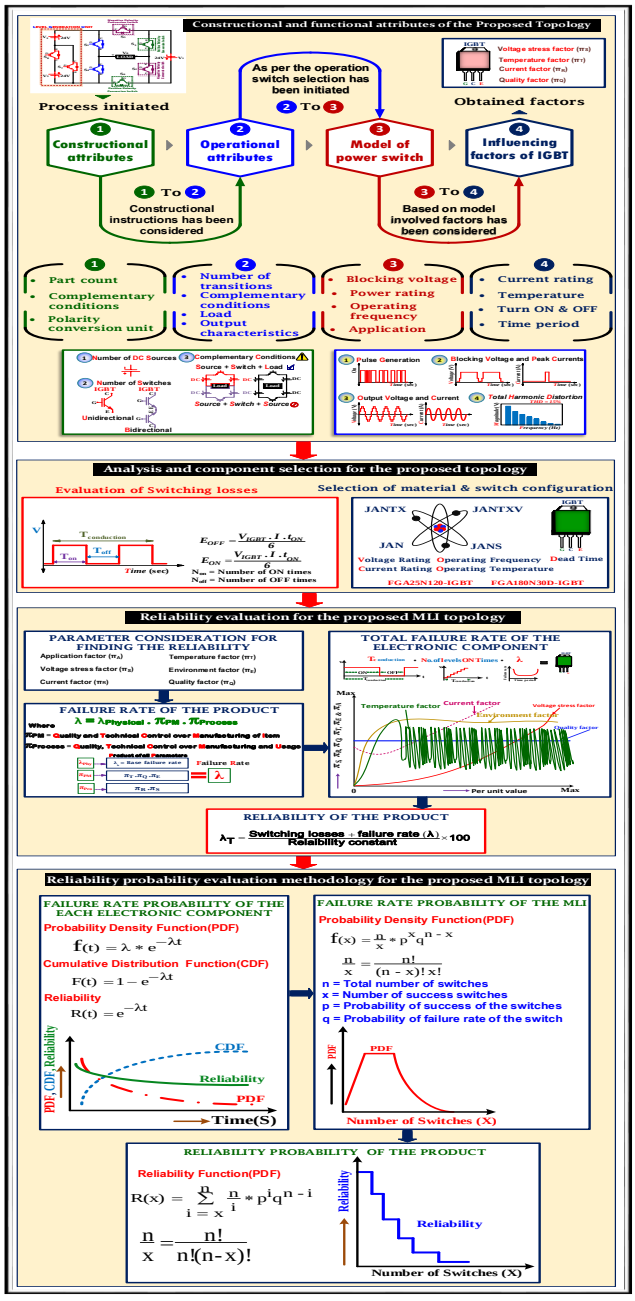


Fig. 2 Process adopted for the reliability estimation of power semiconductor device.

The above methodologies are applicable for the real data of MLI either simulation or hardware but not for the prediction as per the real data. Moreover, the possibilities of the failure prediction with vector quantity of parameters cannot be implemented. Mostly the operation of power semiconductor

devices involves a variety of transitions which can lead to the temperature variations with the addition of environmental temperature. In this case the evaluation of the reliability should support the extension of failure estimation at dynamic conditions. These conventional methodologies are not applicable for extensive reliability analysis, but the proposed methodology can provide the reliability of the product with the integration of historical and experimental data. The advantageous feature of the proposed topology is that the vulnerability of the high operation components failure rate and reliability estimation can be possible with integrated failure data in terms of probability functions. The evaluation of the reliability has been initiated as per the process shown in Fig. 2. According to the proposed reliability methodology has been implemented for MLI topologies as shown in Fig. 2. The general review of the MLI topologies has been performed in next chapter III.

III. REVIEW OF EXISTING TOPOLOGIES

From the analysis of the conventional inverters, researchers have claimed that the level increment in output voltage will lead to more power semiconductor devices procurement to develop the MLI. As a solution towards this problem, MLI topologies have been introduced by the researchers to reduce the power semiconductor devices. The seven-level output voltage has been considered as a common platform to perform the review on MLI topologies in this work. The researchers have introduced the MLI topologies with the different module configuration involving unidirectional and bidirectional switch combinations. In this section, from constructional viewpoint, MLI topologies have been enlisted as with and without bidirectional switch combination and the topologies are as shown in Fig. 3 and Fig. 4.

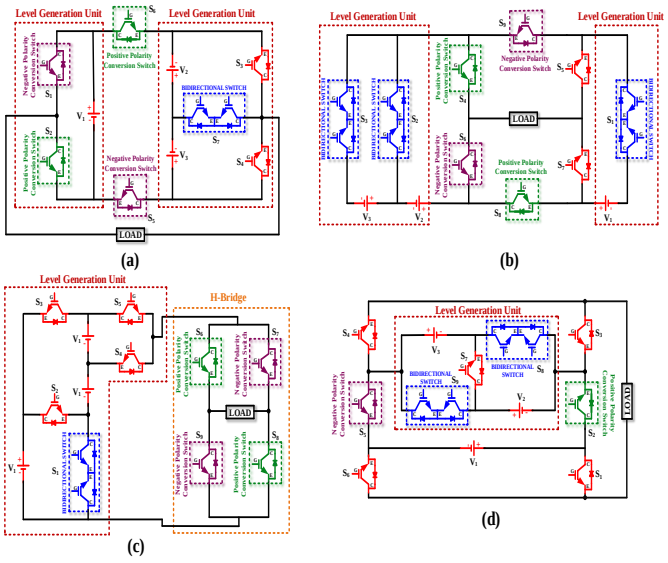


Fig. 3 (a) Topology I proposed in [26] (b) Topology II proposed in [27] (c) Topology III proposed in [28] (d) Topology IV proposed in [29].

In [26]-[29], different types of symmetric topologies have been proposed in Fig.3. Each topology has unique considerations based on the constructional and power semiconductor device configuration. From Fig. 3 it can be observed that all topologies structure involves three DC sources (V_1, V_2, V_3), unidirectional and bidirectional switches (S_1, S_2, S_3…, S_n). Mainly the bidirectional switches are of two types, common collector (CC) and the common emitter (CE). Among these two, CC type has comparatively higher switching losses and two drivers are required to turn-on the switch whereas, CE type requires only single gate driver to turn-on the switch. Because of the advantageous properties of CE type, in Fig. 3 all topologies are configured with the CE bidirectional switch combination. Topology II has been designed with a greater number of bidirectional switches than the other topologies. The level generation units of all the topologies have been configured with the bidirectional switches with different structural features. The bidirectional switch has been operated with the series or parallel connection of the DC source in the generation unit as shown in Fig 3. Topologies I and III require a greater number of switches to make the capable level generation unit for 7-levels in the output voltage. Topology III can generate the +ve and -ve polarity with the H-bridge but the other topologies can generate without H-bridge. It can be observed that the topologies I, II and III involve four switches for generating one cycle but topology IV involves only two switches.

According to the number of switches involved in the generation of the output voltage, topology I involves lesser switches compared with all other topologies as shown in Fig. 3. As per the constructional features of the topologies, topology III has been configured with lesser complementary conditions to perform the expected output generation than the other topologies. Mainly the unidirectional switches are suitable for low power applications and bidirectional switches are suitable for higher power applications, but these topologies are designed with the combination of unidirectional and bidirectional switches. The presence of bidirectional switch can generate the output voltage levels but the switch configuration should be compatible with the other switches, which is a vital factor in the view of implementation. The improper selection of the bidirectional switches will lead to the loss of output and compatibility issues in driver circuit to operate the power switches. For high power applications many conventional topologies involve a combination of unidirectional and bidirectional switches. During real time implementation the surges involved with the bidirectional switch operation may lead to the failure of unidirectional switch involved in the path. This pulls down the reliability of the inverter module. Hence the selection of rating and compatible components involved with the inverter design is a challenging task from field point of view. To achieve a better performance and reduction of implementation difficulties, MLI topologies have been introduced without bidirectional switch as shown in Fig. 4.

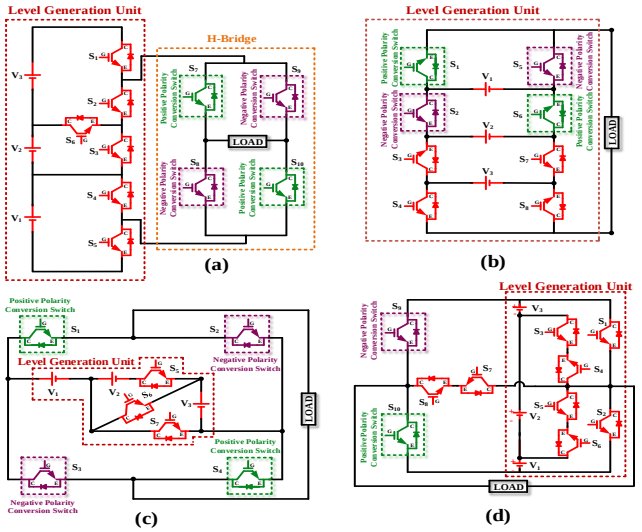


Fig. 4 (a) Topology V proposed in [30] (b) Topology VI proposed in [31] (c) Topology VII proposed in [32] (d) Topology VIII proposed in [33].

Here, 7-level symmetric MLI without bidirectional switch topologies are discussed, which are proposed in [30]-[33], as shown in Fig. 4. The level generation unit of all topologies have been designed with the help of three DC sources (V_1, V_2, V_3) and unidirectional switches (S_1, S_2, S_3,…S_n). The structure of level generation unit has been designed with the series-parallel combination of DC sources and switches to generate the output voltage in all topologies.

From Fig. 4, it can be observed that the level generation units of topology V and VII have been operated with H-bridge to generate the +ve and –ve polarities in output voltage. The topology VIII is capable to generate +ve and –ve polarities with two switches but four switches are required for other topologies. In topology VII the cross connected level generation module has been employed in mid-point section of the H-bridge. The cross connected switch S_6 have made the two cross loops (V_2-S_5-S_6) and (V_3-S_6-S_7). These cross loops may lead to the circulating currents in the level generation unit. Topology VI is also having the circulating current issues because of the DC sources placement between series connected switch combination as shown in Fig. 3. In topology V circulating currents have been eliminated with the required series-parallel connections of switches and DC sources. According to the constructional features, topology VII has lesser complementary conditions than the other topologies but circulating currents may have adverse effects on the operation. It can be concluded that topology VII has advantageous configurational features in the view of part count and topology V has advantageous features in the view of circulating current development possibility. According to the constructional review of MLI topologies, it is evident that the compatibility issues of bidirectional switch with unidirectional switch combination, part count in level generation unit, cross switched module presence, circulating current, and implementation difficulties are highly influencing factors in the constructional configuration of the MLI. Based on this exhaustive examination, a new reliable MLI has been proposed in this work by considering all the above listed factors of major concern.

IV. Proposed Topology

A. Constructional specifications of the proposed topology

In this section new symmetric MLI topology has been introduced with the unidirectional switch configuration to generate the 7-level output voltage. The constructional design of the topology has been structured with the eight switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7, & S_8) and three DC sources (V_1, V_2, & V_3) as shown in Fig. 5. The recent inventions of 7-level MLI topologies constructional and operational attributes have been quantitatively analyzed. For better understanding, the topologies have been simulated in the environment of MATLAB/Simulink with same operating conditions.

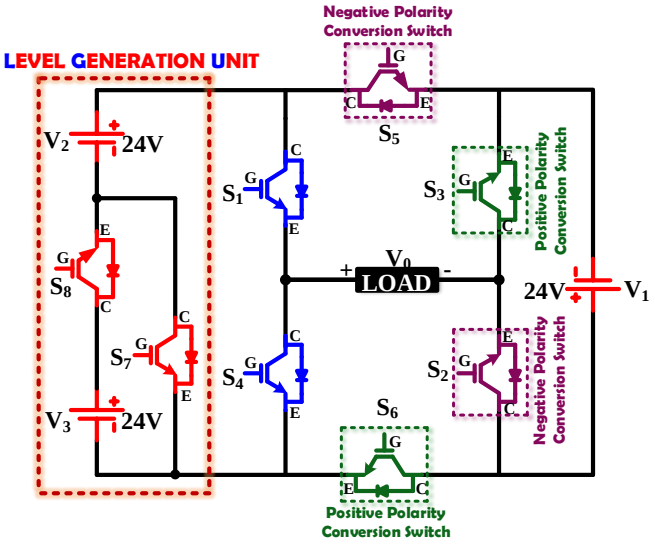


Fig. 5 Proposed structure of the 7-level symmetric MLI topology.

From Fig. 5, it is observed that two switches (S_7 and S_8) and DC sources (V_2 and V_3) are employed in level generation unit with series-parallel combination for the 7-level generation. Four switches (S_2, S_3, S_5, & S_6) are employed to perform the +ve and –ve polarity conversion in output voltage. According to the constructional features of the proposed topology it involves four complementary conditions. The simultaneous turn on of the (S_1, S_4), (S_2, S_3), (S_5, S_6) and (S_7, S_8) will result in voltage source short circuit. The evaluation of constructional equipment procurement has been tabulated in Table I. It can be observed that topologies I and VII involve lesser number of switches compared with the other topologies, but bidirectional switch has been involved in the output generation of the topology I. The complementary conditions of topologies I and VII are same but the circulating current presence plays as an ill effect on topology VII.

TABLE I
CONSTRUCTIONAL FORMULATION DETAILS OF THE TOPOLOGIES

Topology 7-level	Literature	Number of DC sources (N_{DC})	Number of unidirectional switches ($N_{U.Switch}$)		Number of bidirectional switches ($N_{B.Switch}$)		Circulating current paths	Complementary conditions	Total part count
With bidirectional switch	Topology I [26]	$N_{B.Switch}+2$	$N_{level}-1$	6	$N_{level}-N_{U.Switch}$	1	–	9	7
	Topology II [27]	$N_{B.Switch}$	$N_{level}-1$	6	$\frac{N_{U.Switch}}{2}$	3	–	10	9
	Topology III [28]	$N_{B.Switch}+2$	$N_{level}+1$	8	$N_{U.Switch}-N_{level}$	1	–	8	9
	Topology IV [29]	$N_{B.Switch}+1$	N_{level}	7	$\sqrt{\frac{N_{U.Switch}+1}{2}}$	2	–	11	9
	Topology V [30]	$N_{U.Switch}-N_{level}$	$N_{level}+3$	10	–		–	10	10
Without bidirectional switch	Topology VI [31]	$(N_{U.Switch}-N_{level})+2$	$N_{level}+1$	8	–		–	12	8
	Topology VII [32]	$N_{U.Switch}-4$	N_{level}	7	–		✓	9	7
	Topology VIII [33]	$N_{U.Switch}-N_{level}$	$N_{level}+3$	10	–		✓	9	10
	❖Proposed Topology	$(N_{U.Switch}-N_{level})+2$	$N_{level}+1$	**8**	–		–	**4**	**8**

Even topology VI can generate 7-level output voltage without any bidirectional switch and circulating currents, but the complementary conditions are the major challenges from implementation perspective. The above issues have been well taken in the proposed topology. The proposed topology seems to be a reliable one with eight switches, lesser complementary conditions and zero circulating currents. Table I concludes that the proposed topology has been configured with better constructional features than all other reviewed topologies.

B. Operational attributes of the proposed topology

In this section, the detailed operation of the proposed topology has been explained. The topology has been operated for 72 V with three DC sources V_1, V_2, and V_3 each of 24 V. Turn-on (1) and turn-off (0) states of the switches have been tabulated in terms of binary as shown in Table II.

TABLE II
SWITCHING STATES OF THE PROPOSED SYMMETRIC 7-LEVEL MLI TOPOLOGY

Level voltages	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_1 = 24V	0	0	1	1	0	1	0	0
V_1+ V_2 = 48V	1	0	1	0	0	1	1	0
V_1+ V_2+ V_3 = 72V	1	0	1	0	0	1	0	1
-V_1 = -24V	1	1	0	0	1	0	0	0
-(V_1+ V_2) = -48V	0	1	0	1	1	0	1	0
-(V_1+ V_2+ V_3) = -72V	0	1	0	1	1	0	0	1

According to Table II, the required mode of operations of the proposed MLI has been presented as shown in Fig. 6. It can also be observed that when two or more sources are involved in the operation of the circuit, four switches need to be in the active state. Similarly for single source level generation, it demands three switches to be in active state. The active state of the switches S_7 and S_8 is comparatively lesser than other switches. According to the modes of operation of the proposed topology switching pulses have been generated to perform the expected 7-level operation as shown in Fig.7.

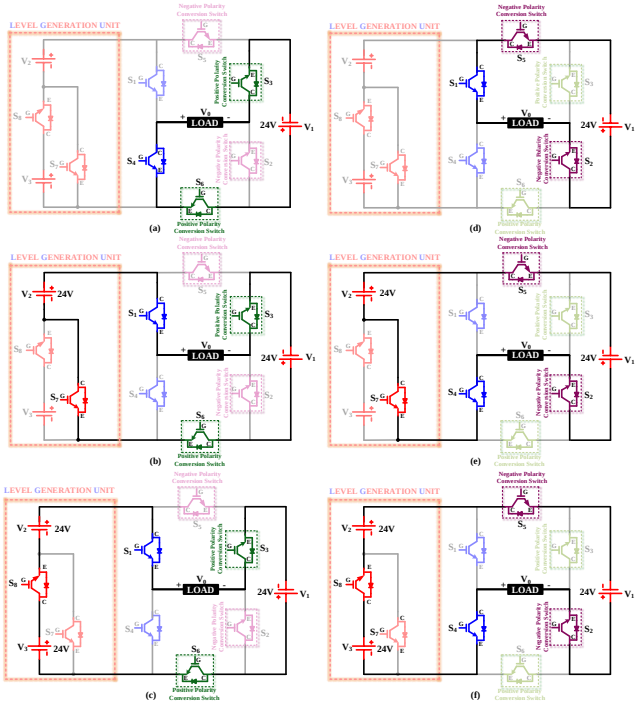


Fig. 6 Equivalent circuits of the level generation (a) Mode-1 (24V) (b) Mode-2 (48V) (c) Mode-3 (72V) (d) Mode-4 (-24V) (e) Mode-5 (-48V) (f) Mode-6 (-72V).

From Fig.7, it is evident that the switching logic involves inherent dead band between the complementary switches. This simplifies the implementation in real time while compared with the other topologies involving more complementary paths. The complementary conditions of the topology will lead to the pulse generation complexity in MLI during real time implementation. According to the switching states of the MLI, the blocking voltage (V_{block}) across each switch is as shown in Fig. 8.

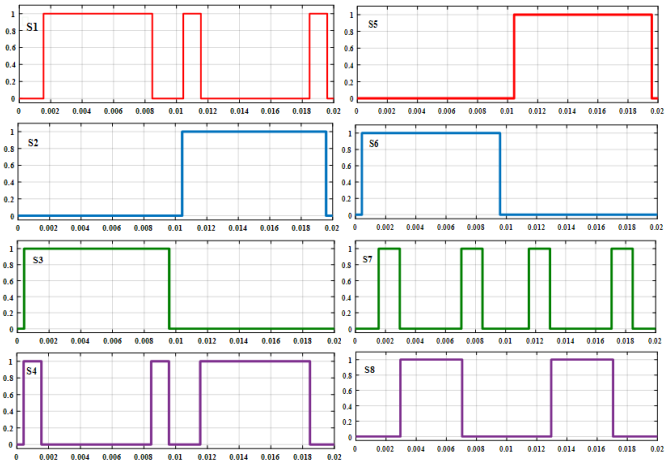


Fig. 7 The required switching pulse of each switch for proposed topology.

Fig. 8 represents the blocking voltage across the individual switch and the addition of all switches blocking voltage is 366 V. But the blocking voltage of the topology is dependent on the particular switches which has been operated for the maximum turn off and on conditions. The main condition to measure the blocking voltage of the topology is to find the maximum voltage blocking nodes in the power circuit along with the power switches. These power switches should perform the maximum turn on and off operation with the total input voltage. In the proposed topology '2' switches (S5 and S6) have been satisfied the condition with the total input voltage of 72 V as shown in Fig. 8. According to this the blocking voltage of the proposed topology is 144 volts and the same is tabulated in the Table 3

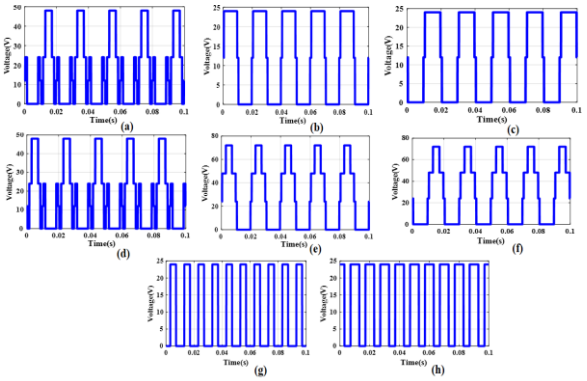


Fig. 8 (a) V_{block} across S_1 (b) V_{block} across S_2 (c) V_{block} across S_3 (d) V_{block} across S_4 (e) V_{block} across S_5 (f) V_{block} across S_6 (g) V_{block} across S_7 (h) V_{block} across S_8.

In addition, the maximum and minimum blocking voltages across the power semiconductor devices are 72 V and 24 V (see Fig. 8). The switches (S5, & S6) are having a maximum blocking voltage, and (S2, S3, S7, & S8) having a minimum range of blocking voltage. The remaining switches (S1, & S4) are having a 48 V range of blocking voltage. Blocking voltage across the various switches is one of the most important factors for the selection of power semiconductor devices and the smooth operation of the MLI. The proposed MLI has been validated in the environment of MATLAB / Simulink and the required results are presented as shown in Fig. 9. In the simulation studies, the proposed topology has been operated with an inductive load, with a value of R = 100Ω and L= 55mH. The pulse generation has been generated as per the logistics of nearest level pulse width modulation technique. It is operated with a switching frequency of 2 kHz and the output voltage frequency of 50 Hz. Fig. 9 (a) ensures that the proposed topology can generate all +ve and –ve levels with the output voltage of 72 V and 1.65 A output current as shown in Fig. 9 (b). The output voltage and current total harmonic distortion (THD) of the proposed topology is shown in Fig. 9 (c) and (d). For better observations about the operational attributes of the proposed topology, quantitative analysis comparison has been performed with the reviewed topologies. The topologies are operated for the total input voltage of 72 V with symmetric source configuration to make the common platform for the operational comparison of the topologies. The quantitative operational attributes of the proposed topology have been compared with the reviewed topologies as shown in Table III.

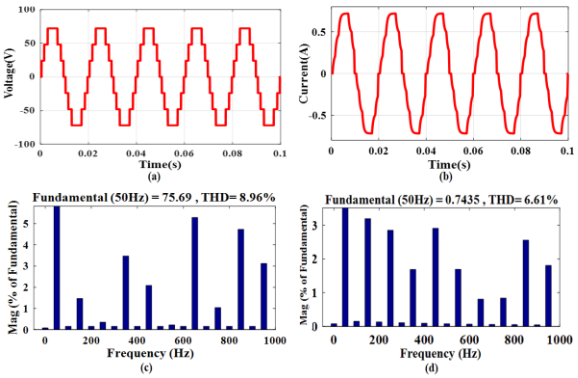


Fig. 9 (a) Output voltage (b) Output current (c) Voltage THD (d) Current THD.

TABLE III
COMPARISON OF OPERATIONAL ATTRIBUTES OF THE PROPOSED TOPOLOGY WITH REVIEWED TOPOLOGIES

S.No	Number of transitions in pulse generation	Blocking voltage (V_{block}) in Volts	THD in %	
			Voltage	Current
Topology I [26]	**23**	**160**	**12.52**	**7.09**
Topology II [27]	**27**	**195**	**9.05**	**6.91**
Topology III [28]	29	228	14.06	8.82
Topology IV [29]	31	260	13.70	7.08
Topology V [30]	36	270	13.66	7.06
Topology VI [31]	24	187	11.91	7.04
Topology VII [32]	**21**	**158**	**13.77**	**7.31**
Topology VIII [33]	**40**	**290**	**14.61**	**8.84**
Proposed Topology	**17**	**144**	**8.96**	**6.61**

From Table III, it can be observed that topology VIII has higher transitions compared with all other topologies and the transitions of the switches is found to have an impact on the blocking voltage of the topologies. It can be concluded from Table III that the proposed topology has been operated with lesser transitions and blocking voltage than all other topologies. The current THD offered by the proposed topology is lesser than all other reviewed topologies. Even topology II

can generate the output current with minimal THD but involves higher transitions and blocking voltage than the proposed topology. It can be concluded that the proposed topology has better operational features compared with the other topologies as shown in Table III. From the above constructional and operational analysis, the proposed topology seems to have better features which in turn has a scope of reduction in switching losses. To quantitatively substantiate this, in the next section the performance analysis of the topologies has been evaluated in terms of switching losses and reliability.

V. The Performance Assessment of the Topologies in terms of Switching losses and Reliability

The performance of the MLI is dependent on the losses development in power switches while operating the topology. The switching losses development is dependent on the turn-on and off times of the switches. But before evaluation process of the switching losses, it is necessary to understand the individual turn-on times of the switches in all the topologies. The turn-on times of the switches in each topology has been obtained from the respective switching table of the topologies. The comparison of the individual turn-on times of the switches in each topology is presented in Fig. 10.

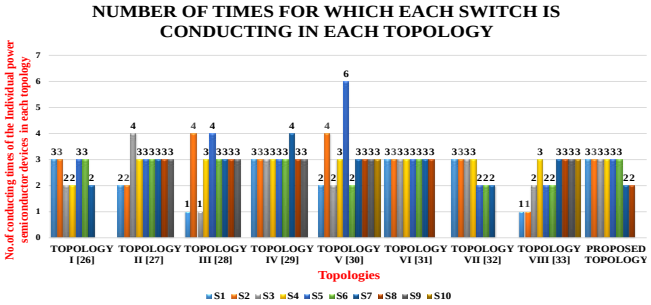


Fig. 10 Switching operation of the Individual switch in each topology.

From Fig. 10, it can be observed that topology V and VIII have more switches than other topologies, but topology V switches have higher turn-on time than all other topologies because of S_2 and S_5 higher turn-on rate. Topologies I and VII have seven switches and lesser turn-on times but the topology I has been configured with the bidirectional switch which may lead to higher switching losses than the topology VII. Topology VI and the proposed topology have eight switches, but turn-on times of the proposed topology is lesser than topology VI. Topology VI has higher turn-on times because of the similar turn-on of the all the switches. The turn-on times have been counted for the evaluation of switching losses of the topologies. Turn ON and OFF process of the power switches is a prime factor for the loss's development and failure possibilities in inverters. Basically, MLI topologies are instructed with higher malfunctions in the process of level generation. Due to this reason, power switches involved in the operation of MLI are suffering from a higher failure rate. According to the above statement, it can be concluded that the reliability of the MLI topologies has been influenced by power semiconductor devices.

It can be observed that the individual losses development in the power semiconductor device is a prime concern to perform the reliability assessment on the MLI topologies. The switching losses development in MLI is one of the performance degrading factors [34]-[36]. The losses development in the power switch depends on the capacity of the blocking voltage and peak current through the device. To evaluate the switching losses, linear profile of the voltage and current have been assumed for the switching operations of each switch [37]-[38]. According to the assumptions, the switching losses development in each switch can be calculated by using the (1) to (3).

Energy loss during turn-on (E_{ON}) and turn-off (E_{OFF})

$$E_{ON} = \frac{V_{IGBT}.I.t_{ON}}{6} \quad (1)$$

Where the V_{IGBT} is the ON-state voltage on the switch, 'I' is the current through the switch after turning on, t_{ON} is the turn-on time of the switch. The energy loss of a switch during E_{OFF} is obtained as follows:

$$E_{OFF} = \frac{V_{IGBT}.I.t_{OFF}}{6} \quad (2)$$

Where the V_{IGBT} is the OFF-state voltage on the switch, 'I' is the current through the switch before turning off, t_{OFF} is the turn-off time of the switch. Based on the switching frequency the number of turn-on (N_{on}), and number of turn-off (N_{off}) switching operations in a fundamental cycle T is decided. The power switching losses can be obtained as follows:

$$\text{Power switching losses} = \frac{1}{T}(N_{on}E_{ON} + N_{off}E_{OFF}) \quad (3)$$

From (1)-(3), switching losses has been evaluated for all topologies and the quantitative analysis of the switching losses have been compared with the proposed topology tabulated in Table IV. The total switching losses of the proposed topology has been estimated in terms of percentage (%) of the total losses by following (4). The losses profile of the MLI is dependent on the number of switches involved in the configuration, and the operating frequency (f_{range}) for a particular time period. According to that, the losses have been evaluated.

$$\left(\frac{\text{Sum of the individual switching lossees (W-sec)}}{\text{Minimum operating time in sec}}\right) * \left(f_{range}\right) * 100 \quad (4)$$

Table IV summarizes quantitatively the losses involved in each topology with respect to each device. Here, it is observed that the topology I, II, III, and IV, the switching losses have been influenced by the operational conditions of bidirectional switches. It can be observed that the unidirectional switches are producing lesser losses compared with the bi-directional switches. Among all, topologies II and III have more switching losses due to higher bidirectional switch count.

TABLE IV
SWITCHING LOSSES OF EACH DEVICE IN ALL THE TOPOLOGIES

S. No	S_1 W-Sec	S_2 W-Sec	S_3 W-Sec	S_4 W-Sec	S_5 W-Sec	S_6 W-Sec	S_7 W-Sec	S_8 W-Sec	S_9 W-Sec	S_{10} W-Sec	Total switching losses in %
Topology I [26]	0.0481	0.0237	0.0136	0.0136	0.144	0.1039	**0.217**	-	-	-	56.39%
Topology II [27]	**0.139**	**0.112**	**0.32**	**0.0630**	**0.0106**	**0.0467**	**0.0158**	**0.0712**	**0.0701**	-	**84.84%**
Topology III [28]	**0.0072**	**0.193**	**0.0011**	**0.1659**	**0.2014**	**0.0713**	**0.0731**	**0.0713**	**0.0731**	-	**85.74%**
Topology IV [29]	0.0193	0.0713	0.0273	0.0267	0.0701	0.083	0.099	**0.226**	**0.114**	-	73.67%
Topology V[30]	0.0170	0.153	0.00089	0.0017	0.275	0.0024	0.0712	0.074	0.071	0.079	74.51%
Topology VI [31]	**0.0437**	**0.0949**	**0.1290**	**0.067**	**0.0437**	**0.0949**	**0.103**	**0.136**	-	-	**71.22%**
Topology VII [32]	**0.0713**	**0.0701**	**0.0701**	**0.0713**	**0.0164**	**0.037**	**0.018**	-	-	-	**35.42%**
Topology VIII [33]	0.0632	0.0327	0.0106	0.038	0.079	0.079	0.144	0.144	0.058	0.029	67.75%
Proposed Topology	**0.042**	**0.035**	**0.0359**	**0.0282**	**0.053**	**0.051**	**0.0029**	**0.0093**	-	-	**25.73%**

In topology II, the maximum individual switching losses is obtained as 0.32 W-Sec. Even though topology III has been configured with lesser bidirectional switches than topology IV, the presence of circulating currents influences the switching losses. According to the observations from Table V, the bidirectional switch configured topologies suffer with more switching losses than other topologies. From Table IV, it is evident that the proposed topology provides lesser switching losses compared with all other topologies. Because the maximum individual loss has been limited to 0.053 W-sec, which leads to the overall reduction in the total losses. Even though topology VII has been operated with lesser switches than the proposed topology but circulating currents have an impact on the switching losses. Topology VI and the proposed topology have been configured with similar part count (eight switches) but topology VI has higher switching losses than the proposed topology because of the higher transitions. It can be concluded that the switching losses of the topology depends on the number of transitions, circulating current development and part count.

From Table IV, it is concluded that the proposed topology is better than other topologies in the view of switching losses profile. In MLI switching losses is one of the factors to decide the performance but the life of the devices is also a major concern, which means the failure rate of the devices. The failure rate of the devices will influence the reliability of the MLI. Thus, the reliability evaluation has been performed for all topologies. Mainly the reliability assessment is dependent on the selection of the material, reliability parameters and ratings of the devices. The reliability of the MLI is dependent on the operational characteristics, specifications, and sensitive parameters of the power semiconductor devices [39]. To initialize the reliability assessment JANTX material has been considered for the power semiconductor selection [40]-[41]. The reliability assessment methodology has been followed as per Fig.10 to find the reliability of the topologies in terms of the failure rate of the power semiconductor devices. The required sensitive parameters for the evaluation of the failure rate of power semiconductors have been considered as per the standards of the Mil-Hdbk-217F [42]. The voltage stress (π_S), current (π_R), quality (π_Q), temperature (π_T), environmental (π_E), application (π_A), and material constant factors have been considered to evaluate the reliability of the power semiconductor devices in terms of failure rate. The failure rate is defined as the product of the physical failure $(\lambda_{Physical})$, quality control (π_{PM}) and manufacturing material usage $(\pi_{Process})$. It is denoted by 'λ'. The necessary formulae for evaluating the failure rate are given from (5) to (8).

$$\lambda = \lambda_b \quad \text{Where } \lambda_b = \text{Failure rate} \tag{5}$$

The failure rate of the product

$$\lambda = \lambda_{Physical} * \pi_{PM} * \pi_{Process} \tag{6}$$

$$\pi_{PM} = \pi_T . \pi_Q . \pi_E \tag{7}$$

$$\pi_{Process} = \pi_R . \pi_S \tag{8}$$

The selection of the power semiconductor device is the most important factor to find the reliability of the MLI. According to the operational characteristics of all the MLI topologies, the configured switch model has been selected to implement the reliability methodology. The configuration specifications of the switch model have been tabulated in Table V.

TABLE V
CONFIGURATIONAL SPECIFICATIONS OF THE POWER SEMICONDUCTOR DEVICE

Model of the switch	Specifications of the switch configuration			
	Voltage rating (V)	Current rating (A)	Junction temperature (°C)	Selected Material
FGA180N30D	300	30	150°	JANTX

According to the configuration details of the power semiconductor device from Table V, the individual failure rate of each device for the all topologies have been evaluated by using the (5)-(8). The failure rate of the individual switch in all topologies are tabulated in Table VI. Mainly the failure rate of the power semiconductor is dependent on the even participation in the number of transitions for a particular time period with the considerations of current (π_S) and voltage (π_R) to perform the operation. From Table VI it is concluded that the bidirectional switched configured topologies are suffering with greater failure rate than unidirectional switched configuration topologies. In the bidirectional switched configured topologies, even the unidirectional switch taking part in the forward conduction mode seems to suffer with higher failure rates, due to the peak currents or circulating currents involved with the operation. In topology VIII the individual switch failure rate is higher with the maximum failure rate of 0.9013 per 10^6 hours compared with all other topologies.

TABLE VI
FAILURE RATE OF EACH DEVICE IN ALL TOPOLOGIES

S. No	S_1 $\lambda/10^6$ hours	S_2 $\lambda/10^6$ hours	S_3 $\lambda/10^6$ hours	S_4 $\lambda/10^6$ hours	S_5 $\lambda/10^6$ hours	S_6 $\lambda/10^6$ hours	S_7 $\lambda/10^6$ hours	S_8 $\lambda/10^6$ hours	S_9 $\lambda/10^6$ hours	S_{10} $\lambda/10^6$ hours	Total failure rate of the MLI 10^6 hours
Topology I [26]	0.4506	0.4506	0.6004	0.6004	0.4506	0.4506	0.3004	-	-	-	3.3036
Topology II [27]	0.3004	0.3004	0.6009	0.4506	0.4506	0.4506	0.4506	0.4506	0.4506	-	3.9053
Topology III [28]	0.1502	0.6009	0.1502	0.4506	0.6009	0.4506	0.4506	0.4506	0.4506	-	3.7567
Topology IV [29]	0.4506	0.4506	0.4506	0.4506	0.4506	0.4506	0.6009	0.3502	0.4502	-	4.1049
Topology V [30]	0.1502	0.1502	0.3004	0.4506	0.3004	0.3004	0.4506	0.4506	0.1502	0.1502	2.8541
Topology VI [31]	0.4506	0.4506	0.4506	0.4506	0.4506	0.4506	0.4506	0.4506	-	-	3.6048
Topology VII [32]	0.4506	0.4506	0.4506	0.4506	0.3004	0.3004	0.3004	-	-	-	2.7036
Topology VIII [33]	0.3004	0.6009	0.3004	0.1502	0.9013	0.3004	0.4506	0.4506	0.4506	0.4506	4.3563
Proposed Topology	**0.240**	**0.240**	**0.240**	**0.240**	**0.3004**	**0.3004**	**0.024**	**0.034**	**-**	**-**	**1.6188**

Topology V and VIII have been configured with similar part count but the topology VIII has higher individual switch failure rate because of the higher transitions and circulating current development. From Table VI, it can be observed that the failure rate of the individual switch in proposed topology is lesser compared with all other topologies. Even topology VII has been configured with the lesser number of switches than the proposed topology, but topology VII has higher failure rate due to the circulating currents and higher transitions. Topology VI and proposed topology has been configured with the similar part count, but the failure rate of the topology VI is higher than the proposed topology because of the higher transitions.

TABLE VII
THE RELIABILITY OF THE ALL TOPOLOGIES

S. No	Switching losses (W-Sec) of the MLI in %	Failure rate of the MLI (λ_T) 10^6 Hours	Reliability of the MLI in terms of failure rate in %
Topology I [26]	56.39%	3.3036	38.675%
Topology II [27]	84.84%	3.9053	**47.537%**
Topology III [28]	85.74%	3.7567	**46.141%**
Topology IV [29]	**73.67%**	**4.1049**	**48.416%**
Topology V [30]	74.51%	2.8541	35.992%
Topology VI [31]	71.22%	3.6048	**43.17%**
Topology VII [32]	35.42%	2.7036	30.578%
Topology VIII [33]	**67.75%**	**4.3563**	**50.338%**
Proposed topology	**25.73%**	**1.6188**	**18.761%**

From table VI, it can be concluded that the presence of bidirectional has an impact on power semiconductor devices peak current in MLI and this is well proven from the failure rate figures of the topology I, II, III and IV. Also, from the same table, it is evident that higher circulating currents and a greater number of transitions have influence on the failure rate of the switches, and this has been confirmed with the analysis of individual switch failure rate figures of topology V, VI, VII and VIII. From the exhaustive analytical investigation, the proposed topology sounds to be a promising one with lesser switching losses and failure rate when compared with all other existing counterparts.

The quantitative analysis of the operational characteristics and failure rate profile of each topology has been considered to find the reliability of each topology. Because the reliability evaluation of the MLI is dependent on the operational characteristics and failure rate of the power switches for the specific operation in a particular time. The reliability (λ_T) of the MLI topologies have been evaluated by using (9) and are tabulated in Table VII as shown below.

The reliability of the MLI

$$\lambda_T = \frac{\text{Switching losses} + \text{failure rate}\,(\lambda)}{\text{Relaibilit y constant}} \times 100 \qquad (9)$$

The reliability constant is a vital parameter for power electronics modules. The reliability constant which is less than 1.5 has been considered to find the power circuit reliability of the proposed topology as per the standards of Mil-Hdbk-217F for long run application.

TABLE VIII
DEVICE LEVEL ANNUAL FAILURE RATE FOR THE PROPOSED TOPOLOGY

Annual operations	Different failure rates of the switches in proposed topology (λ)/10^6 Hours					
	Short run operation 6 Hours/day		Medium run operation 12 Hours/day		Long run operation 24 Hours/day	
	S_1, S_2, S_3, S_4, S_5, & S_6	S_7 & S_8	S_1, S_2, S_3, S_4, S_5, & S_6	S_7 & S_8	S_1, S_2, S_3, S_4, S_5, & S_6	S_7 & S_8
3 months (92 days)	**0.0228**	**0.0513**	**0.0513**	**0.0342**	**0.1083**	**0.0722**
6 months (183 days)	**0.0513**	**0.0342**	**0.1083**	**0.0722**	**0.2223**	**0.1482**
12 months (365 days)	**0.1083**	**0.0722**	**0.2223**	**0.1482**	**0.4503**	**0.3002**

From table VII, it can be observed that the switching losses is one of the factors for the performance degradation from the operational aspects and do not have higher impact on the field reliability. But from this detailed evaluation, it can be inferred that the number transitions in each topology have a greater impact on the failure rate. To validate the above statements, topology IV and VIII can be considered which involves lesser switching losses but higher failure rate due to more number of transitions in the operation. Topologies II and III have more switching losses but lesser failure rate which proves that these two factors are trade-offs. The switching losses and failure rate of the product are two important factors from selection point of view. While selecting a topology for a specific application, these two factors are to be fixed based on the trade-off. In order to have a reliable and functional topology, it must be taken care that the switching losses and failure rate are well within the permissible limits.

From Table VII it can be concluded that the proposed topology is found to be the best suitable choice for real time applications in the view of switching losses and failure rate. This topology offers 18.761% of reliability in terms of failure rate compared with all other topologies. For the better picture on the performance analysis of MLI, Table VII data have been presented pictorially in Fig. 11.

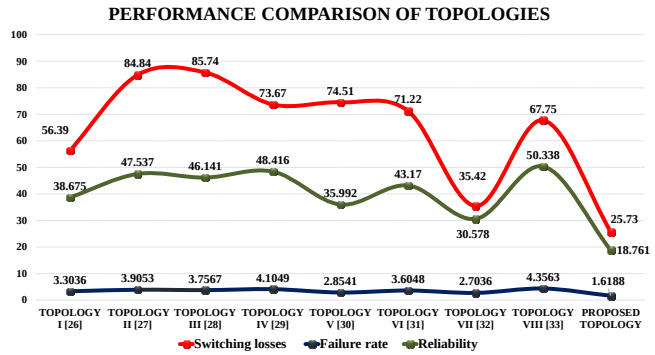


Fig. 11 Performance comparison of the MLI topologies.

From the results, it can be observed that the proposed topology has better performance compared with all other topologies. The proposed topology is providing the better reliability in terms of failure rate with 25.73% of switching losses and 1.61% of failure rate. By considering the constructional, operational, and performance comparison it can be concluded that the proposed topology is better than reviewed topologies for implementation.

The design level reliability is the primary data for the implementation process. The reliability of the product is dependent on the life cycle of the product as well as power semiconductor deployment in the operation [43]. The failure rate of the power semiconductor at different annual operations are as shown in Table VIII. The annual failure rate of the product is dependent on the operating hours of the product [44]. It has been calculated by (10).

$$\text{Annual failure rate} = \sum_{i}^{\text{phase}} \frac{\text{annual time}}{8760} \times \lambda \qquad (10)$$

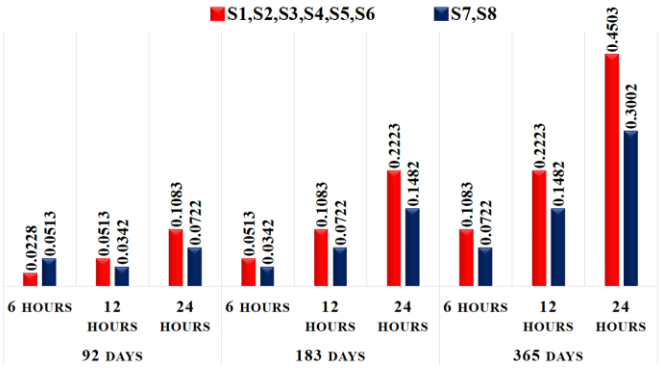


Fig. 12 Annual failure rate of each switch.

Table VIII which provides the quantitative data analysis of annual failure rate (AFR), is a useful information to obtain the probability of each power semiconductor in the proposed topology. The considered maximum individual annual operating time of the switches is 365 days (1 year). For the better understanding the annual failure rate has been explored pictorially as in the Fig. 12. The probability of the power switches has been obtained mathematically using the exponential continuous distribution. The probability reliability of the power switches in terms of failure rate has been calculated by using the formulae (11) to (13) which is as per the standards of [45].

$$\text{Probability density function (PDF)} \quad f(t) = \lambda e^{-\lambda t} \qquad (11)$$

$$\text{Cumulative density function (CDF)} \quad F(t) = 1 - e^{-\lambda t} \qquad (12)$$

$$\text{Probability of reliability} \quad R(t) = e^{-\lambda t} \qquad (13)$$

According to the operation of the MLI, switches have been selected for the required level generation. The parameter variation has an impact on the failure rate of the product. Here temperature of the switch has been considered for finding the reliability of each switch because of π_S, π_R, π_Q, π_E, π_A, and material constant are fixed parameters. Any variations in the π_S, and π_R leads to the higher temperature developments in power semiconductor device. The failure rate of the product at different temperature is as shown in Table IX. The evaluation of the temperature constant for different operating condition has been calculated by the (14).

$$\pi_t = e^{\left(-3082\left(\frac{1}{T_j+273} - \frac{1}{T_r}\right)\right)} \qquad (14)$$

The junction temperature (T_j) plays a vital role in the process of π_T determination. The failure rate of the switch has been calculated by the various Tj at the ideal room temperature (T_r) 25°c.

TABLE IX
IMPACT OF TEMPERATURE ON THE DEVICE LEVEL FAILURE RATE

Junction Temperature T_j (c)		Device level failure rate of proposed topology (λ)/10^6 Hours							
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Low	30°	0.02	0.02	0.02	0.02	0.02	0.02	0.01	0.01
	60°	0.05	0.05	0.05	0.05	0.05	0.05	0.03	0.03
Medium	90°	0.10	0.10	0.10	0.10	0.10	0.10	0.072	0.072
High	120°	0.22	0.22	0.22	0.22	0.22	0.22	0.14	0.14
	150°	0.3	0.3	0.3	0.3	0.3	0.3	0.22	0.22

From Table IX, it is observed that the incremental characteristics of the temperature will lead to the product failure. The devices encounter maximum failure rate while operating with the maximum junction temperature of 150°c. According to Table VIII annual failure rate of the devices at different temperatures (AFR_T) have been calculated. The device level annual failure rates have been tabulated in the Table X. The total annual failure rate (TAF) of the switch has been calculated for the long run operation. The failure rate has been evaluated by (15).

$$TFA = AFR + AFR_T \qquad (15)$$

TABLE X
DEVICE LEVEL ANNUAL FAILURE RATE FOR THE PROPOSED TOPOLOGY

S.no Devices	Device annual failure rates of the each switch in proposed topology (λ)/10^6 Hours														
	92 days (24H/day)					183 days (24H/day)					365 days (24H/day)				
	30°	60°	90°	120°	150°	30°	60°	90°	120°	150°	30°	60°	90°	120°	150°
S_1, S_2, S_3, S_4, S_5, & S_6	0.128	0.158	0.208	0.328	0.408	0.242	0.272	0.322	0.442	0.522	0.470	0.500	0.550	0.670	0.750
S_7 & S_8	0.082	0.102	0.144	0.212	0.29	0.158	0.158	0.22	0.288	0.368	0.310	0.330	0.372	0.440	0.52

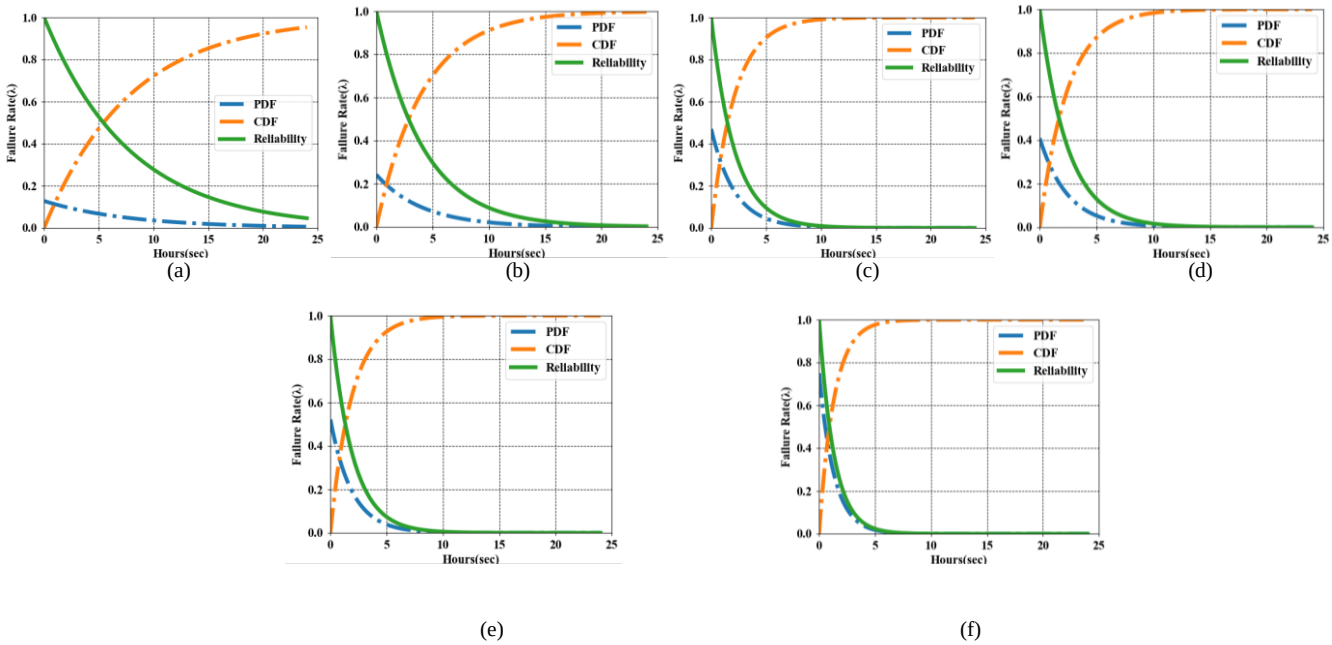


Fig. 13 Device level probability reliability of the switches in the proposed topology at different temperatures and annual times (a) 92 days at T_j of 30°c (b) 183 days at T_j of 30°c (c) 365 days at T_j of 30°c (d) 92 days at T_j of 150°c (e) 183 days at T_j of 150°c (f) 365 days at T_j of 150°c.

It can be observed from Table X that the annual time and the operating temperature will have an impact on the failure rate. In the proposed topology S_1, S_2, S_3, S_4, S_5, and S_6 switches are providing the maximum failure at different temperatures compared with other switches S_7, & S_8. According to the total annual failure rate of the switches the probability distribution has been applied to find the reliability probability of the switches. For probability estimation, the most vulnerable switches with maximum failure rate have been considered. The probability reliability of the switch has been arrived by using (11) to (13). The device level probability reliability is as shown in Fig. 13.

The reliability estimation of the switches in the proposed topology has been performed in terms of failure rate over a particular time period or annual operation. The failure of the power semiconductor depends upon the switching times. The annual operating time of the product influences the lifetime of the product. The impact of the annual time and failure rate on the switches can be observed form Fig. 13. Fig. 13. (a), (b) and (c) represents the probability reliability estimation of the switches at a T_j of 30°c and (d), (e) and (f) represents the probability reliability estimation of the switches at a T_j of 150°c. It can be observed that increment in the annual operating time leads to higher failure rate of the switch. The probability reliability of the switches has been used for finding the system reliability. The evaluation process of the system probability reliability has been performed by the method of binomial distribution. The evaluation of probability reliability of the system has been evaluated by using the necessary formulae from (16) to (20), as per the standards of MIL-HDBK-338B [46]-[47].

$$\text{Probability density function (PDF)} \quad f(x) = \binom{n}{x} p^x \, q^{n-x} \qquad (16)$$

$$\text{Where} \binom{n}{x} = \frac{n!}{(n-x)!\, x!}, \qquad q = 1-p \qquad (17)$$

Cumulative density function (CDF)

$$R(x) = \sum_{i=x}^{n} \binom{n}{x} q^x \, p^{n-x} \qquad (18)$$

$$\text{Where} \binom{n}{x} = \frac{n!}{n!(n-x)!}, \qquad q = 1-p \qquad (19)$$

n = Total number of switches, x = Number of success switches, p = probability of success of the switches, q = probability of failure rate of the switch.

Reliability function $F(t) = 1 - R(x)$ (20)

According to the operation of the MLI two switches are involved in more complimentary conditions compared with the other six switches. The most allowable failure chances of the system are 2. Accordingly, the probability reliability of the system has been estimated without loss of more than two switches is as shown in Fig. 14.

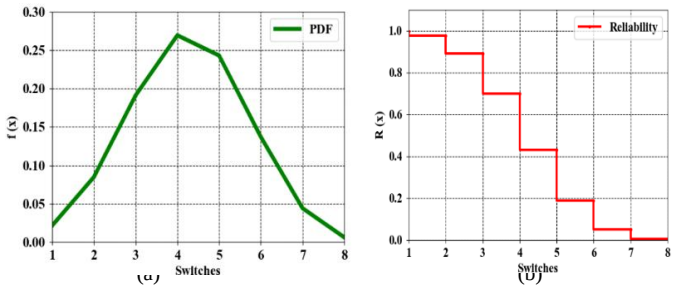


Fig. 14 (a) Probability of the switches failure rate (b) Probability reliability of the system.

From Fig. 14 (a), according to the failure rate probability of the switches, the maximum failure rate is obtained as two switches at the worst-case operation. The relation between the switches and reliability of the MLI can be observed from Fig. 14. (b). The reliability of the MLI is dependent on the failure of the switches. It can be observed from Fig. 14. (b), that the reliability of system is greatly influenced by the number of switch failures. The proposed topology is capable to provide the 21.01% of system reliability in terms of failure rate at the worst-case scenario. From the exhaustive assessment and results, it is evident that the proposed topology seems to be a promising circuit for the long run applications like marine, industrial and renewable applications. The long run applications reliability of the proposed topology has been tabulated in Table XI.

TABLE XI
LONG-RUN APPLICATIONS RELIABILITY OF THE PROPOSED TOPOLOGY

Application	Failure rate (λ)/10^6 Hours		Reliability (%)	
	conventional	Proposed method	conventional	Proposed method
Marine	4.993	2.801	56.32%	34.7 %
Industrial	4.631	2.768	54.25%	33.64%
Renewable	4.354	2.131	51.96%	28.5%

From Table XI it can be concluded that the proposed reliability methodology has been provided the better quantitative values of reliability than conventional methods. To exhibit the performance of the proposed topology, it has been validated with the hardware implementation. The implementation details of the proposed topology have been explained in next section.

VI. Hardware Implementation Of The Proposed Topology

In this section, as per the reliability assessment parameters of single phase proposed symmetric 7-level MLI topology, experimental prototype has been implemented as shown in Fig.15. The specifications of devices employed in the experimental prototype are listed in Table XII.

TABLE XII
THE SPECIFICATIONS OF THE DEVICES EMPLOYED IN THE HARDWARE

S. No	Name of the device	Specifications	Quantity
1	1-ϕ Multi tap transformer	230V/16V	1
2	Drivers	15V	8
3	Optocoupler	TLP250	8
4	Arduino Mega	ATmega2560	1
5	IGBT	FGA180N30D	8
6	Resistive load	100Ω	1

The experimental prototype of the proposed MLI has been implemented with the procured components as shown in Fig. 15.

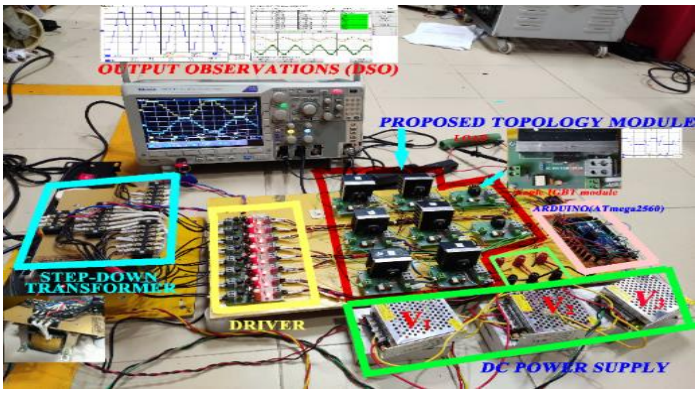
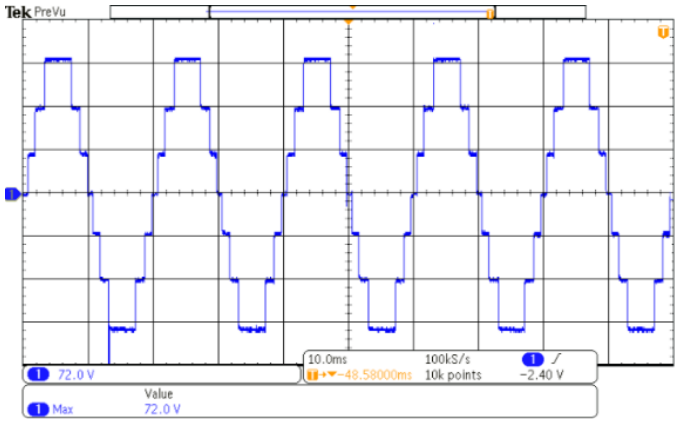
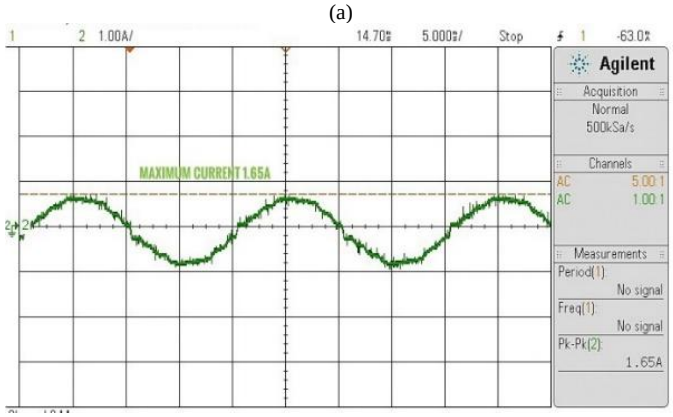


Fig. 15 Experimental prototype of the proposed

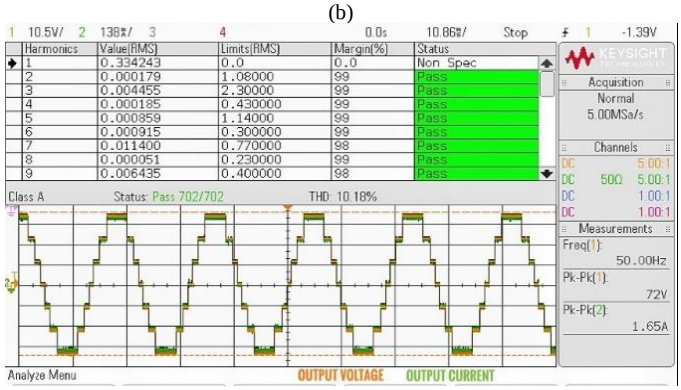
The proposed topology has been operated for input voltage of 72 V with three input DC sources each source of 24 V with R and R-L load of R =100 Ω L =55 mH. The ARDINO MEGA (ATmega2560) has been used to generate the required switching pulse pattern with the switching frequency of 2 kHz. According to the switching pattern and input voltage, the proposed topology has provided the 7-levels output voltage of 72 V and output current of 1.65 A with R and R-L load is shown in Fig. 16 (a) and (b). The distortion in the current arises due to the non-sinusoidal components (harmonics), present in the supply voltage. These components while interacting with the linear impedance will result in a current with same harmonics. Even though the impedance is linear, the applied voltage's non-ideal waveform leads to distorted current waveforms. The I/O characteristics has been observed by using the DSO-X 2002A. Current THD offered by the topology for R-load is 10.18% and R-L load is 7.10% as shown in Fig. 16 (c) and (d). According to the operation of the proposed topology blocking voltage across each switch is as shown in Fig. 16 (e), (f), (g) and (h) and it can be observed that the experimental results of proposed topology are in line with the simulation result. From Fig.16, it can be concluded that the proposed topology is capable to generate the 7-levels in output voltage with THD of 7.01%. Hence the proposed topology is experimentally validated.



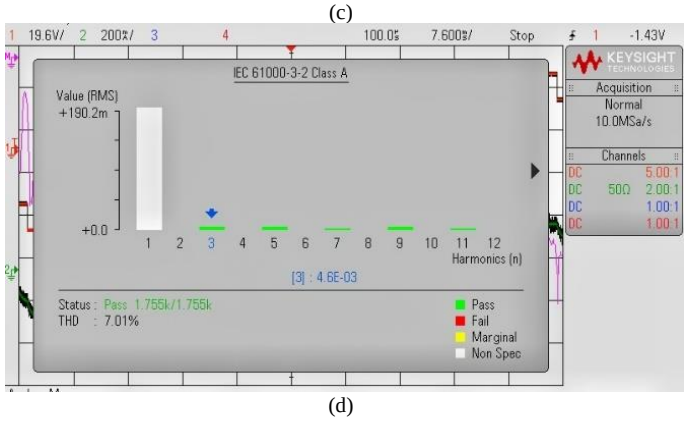
(a)



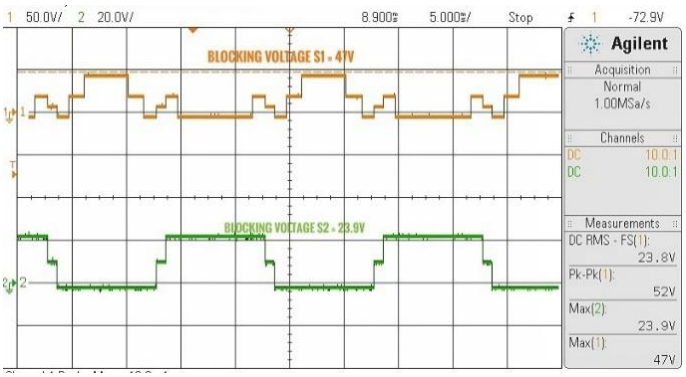
(b)



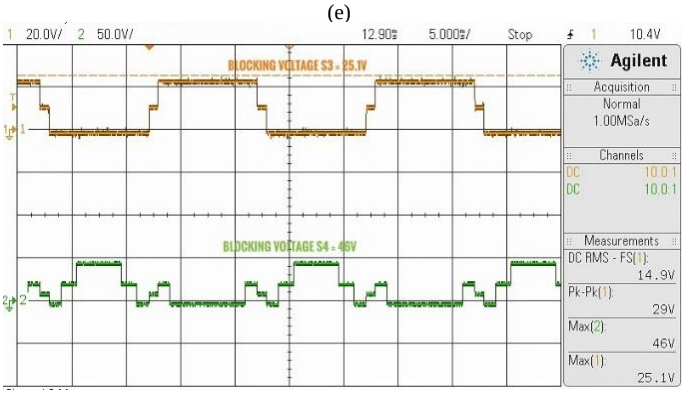
(c)



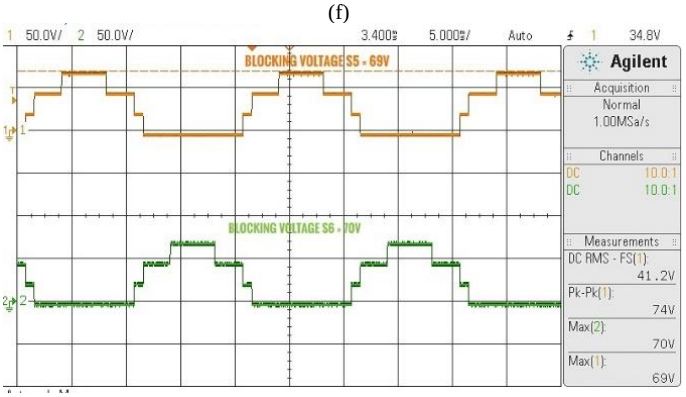
(d)



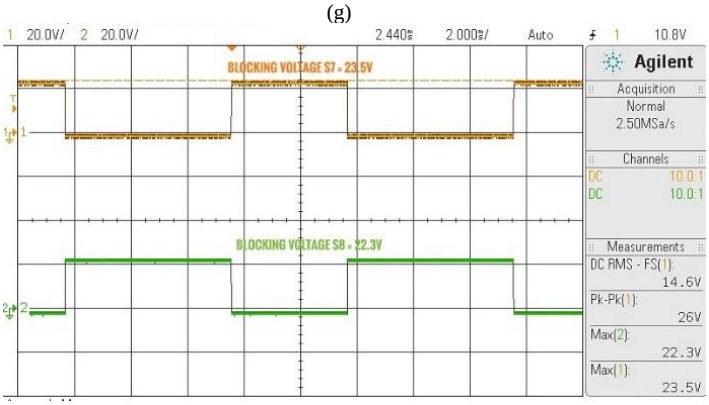
(e)



(f)



(g)



(h)

Fig. 16. Experimental results of the proposed topology (a) Output voltage(b) Output current (c) Current THD with R-load (d) Current THD with RL-load (e) V_{block} of S_1 and S_2 (f) V_{block} of S_3 and S_4 (g) V_{block} of S_5 and S_6 (h) V_{block} of S_7 and S_8.

VII. CONCLUSION

According to the detailed investigations, it is evident that symmetric MLI topologies have superior attributes from constructional, operational and implementation perspectives than asymmetric topologies. This work has compiled the constructional and functional performance of the recent eight symmetric MLI topologies in various aspects. Based on the observations a new MLI topology has been proposed with lesser number of transitions (17), complementary conditions (4), THD (6.61%), and switching losses (25.73%) while comparing with all other existing topologies. To aid the designers, a new reliability evaluation process has been proposed for MLI topologies. Using this new reliability evaluation process the individual power switch reliability and the topological reliability has been estimated for all the reviewed topologies and the proposed topology. From the quantitative results of reliability, the following conclusions have been deduced:

- The number of transitions and circulating currents have a higher impact on the failure rate of the switches rather than the switching losses. For instance, topology III with the highest switching losses (85.74%) is not yielding the highest failure rate (3.7567) 10^6 hours. But the topology VIII with the highest possible number of transitions (40) suffers with the highest failure rate (4.3563) 10^6 hours. As an added feature this proposed topology involves no circulating currents and offers an acceptable failure rate (1.6188) 10^6 hours which ensures favorable real time implementation.
- As per the comparison of performance parameters of the all the topologies it can be concluded that the proposed topology has been featured with the better reliability of 18.761% in terms of failure rate. According to the operational attributes of the proposed topology it can be observed that level generation unit switches S7 and S8 are involved with lesser failure rate than all other switches.
- Due to the unequal failure developments in the proposed topology the reliability probability estimation has been performed with concern of annual failure rate. To have a clear picture from field perspective, the reliability has been estimated with the different temperatures of 30°, 60°, 90°, 120° and 150°c for diverse annual operating periods.
- Form the reliability probability analysis it can be concluded that the proposed topology is suitable for long run applications. The reliability of the proposed topology for long run applications of marine 34.7%, industrial 33.64%, and renewable 28.5%.

To validate the contribution, we have presented the hardware implementation of proposed MLI topology along with the necessary results. The new MLI introduced in this work demonstrates superior functionality and reliability, making it a promising candidate for real time applications. Given its enhanced reliability, we can assert that the proposed topology is well-suited for long-run applications.

ACKNOWLEDGMENT

The authors would like to acknowledge the fund support from the Royal Academy of Engineering, UK. Award reference No. TSP-2325-5-IN\172. This work has been carried out in School of Electrical Engineering, Vellore Institute of Technology, Vellore, India.

REFERENCES

[1] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, “Modular multilevel converters for HVDC applications: Review on converter cells and functionalities,” *IEEE Transactions on Power Electronics,* vol. 30, no. 1, pp. 18-36, Jan. 2015.

[2] Q. A. Le and D. C. Lee, “A novel six-level inverter topology for medium voltage applications,” *IEEE Transactions on Industrial Electronics,* vol. 63, no. 11, pp. 7195-7203, Nov. 2016.

[3] M. Narimani, B. Wu, and N. R. Zargari, “A novel five-level voltage source inverter with sinusoidal pulse width modulator for medium-voltage applications,” *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1959-1967, Mar. 2016.

[4] L. Wang, Q. H. Wu and W. Tang, “Novel cascaded switched-diode multilevel inverter for renewable energy integration,” *IEEE Transactions on Energy Conversion,* vol. 32, no. 4, pp. 1574-1582, Dec. 2017.

[5] M. Andresen, V. Raveendran, G. Buticchi, and M. Liserre, “Lifetime based power routing in parallel converters for smart transformer application,” *IEEE Transactions on Power Electronics,* vol. 65, no. 2, pp. 1675-1684, Feb. 2018.

[6] A. Sheir, M. Z. Youssef and M. Orabi, “A novel bidirectional t-type multilevel inverter for electric vehicle applications,” *IEEE Transactions on Power Electronics,* vol. 34, no. 7, pp. 6648-6658, Jul. 2019.

[7] A. Kersten, O. Theliander, E. A. Grunditz, T. Thiringer and M. Bongiorno, “Battery loss and stress mitigation in a cascaded h-bridge multilevel inverter for vehicle traction applications by filter capacitors,” *IEEE Transactions on Transportation Electrification,* vol. 5, no. 3, pp. 659-671, Sept. 2019.

[8] R. S. Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, “Reduction of power electronic elements in multilevel converters using a new cascade structure,” *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 256-269, Jan. 2015.

[9] F. Ebrahimi, N. A. Windarko and A. I. Gunawan, "Reducing THD of 7-Level Packed U-cell Multilevel Inverter Using Genetic Algorithm," *2023 International Electronics Symposium (IES)*, Denpasar, Indonesia, 2023, pp. 88-93, doi: 10.1109/IES59143.2023.10242460.

[10] A. K. Yadav, K. Gopakumar, K. R. R, L. Umanand, S. Bhattacharya and W. Jarzyna, "A Hybrid 7-Level Inverter Using Low-Voltage Devices and Operation With Single DC-Link," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9844-9853, Oct. 2019, doi: 10.1109/TPEL.2018.2890371.

[11] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena and J. Rodriguez, "Voltage Source Multilevel Inverters With Reduced Device Count: Topological Review and Novel Comparative Factors," in *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2720-2747, March 2021, doi: 10.1109/TPEL.2020.3011908.

[12] M. Vijeh, M. Rezanejad, E. Samadaei and K. Bertilsson, "A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9479-9502, Oct. 2019, doi: 10.1109/TPEL.2018.2890649.

[13] R. Barzegarkhoo, M. Forouzesh, S. S. Lee, F. Blaabjerg and Y. P. Siwakoti, "Switched-Capacitor Multilevel Inverters: A Comprehensive Review," in *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 11209-11243, Sept. 2022, doi: 10.1109/TPEL.2022.3164508.

[14] Krishnachaitanya D, Annamalai C. Real time implementation of a new seven level multilevel inverter with design considerations for feasible and reliable operation. Int J Circ Theor Appl. Vol. 51, no. 10, pp. 4839-4863, May. 2023, doi:10.1002/cta.3653.

[14] R. Barzegarkhoo, M. Forouzesh, S. S. Lee, F. Blaabjerg and Y. P. Siwakoti, "Switched-Capacitor Multilevel Inverters: A Comprehensive Review," in *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 11209-11243, Sept. 2022, doi: 10.1109/TPEL.2022.3164508.

[16] C. Terbrack, J. Stöttner and C. Endisch, "Design and Validation of the Parallel Enhanced Commutation Integrated Nested Multilevel Inverter Topology," in *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 15163-15174, Dec. 2022, doi: 10.1109/TPEL.2022.3183859.

[17] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135-151, Jan. 2016.

[18] R. Barzegarkhoo, H. M. Kojabadi, E. Zamiry, N. Vosoughi, and L. Chang, "Generalized structure for a single phase switched-capacitor multilevel inverter using a new multiple DC link producer with reduced number of switches," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5604-5617, Aug. 2016.

[19] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series-parallel conversion with less number of components," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3582-3594, Jun. 2016.

[120] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main sub modules: Structural point of view," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9479-9502, Oct. 2019.

[21] D. T. Do and H. Cha, "High-reliability and reduced switch count single-phase dual-output current source inverter using switching-cell structure," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6513-6524, Jun. 2021.

[22] J.S.M. Ali, and V. Krishnaswamy, "An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications" *Renewable and Sustainable Energy Reviews*, vol. 82, no. 3, pp. 3379-3399, Feb. 2018.

[23] M. Quraan, P. Tricoli, S. D. Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2041-2051, Mar. 2017.

[24] A. K. Yadav, K. Gopakumar, K. R. R, L. Umanand, S. Bhattacharya and W. Jarzyna, "A hybrid 7-level inverter using low-voltage devices and operation with single DC-link," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9844-9853, Oct. 2019.

[25] V. V. Fedotov and V. V. Rozhkov, "Development and Analysis for the Optimal Structure of a Multilevel Voltage Source Inverter," *2021 International Ural Conference on Electrical Power Engineering (UralCon)*, Magnitogorsk, Russian Federation, 2021, pp. 121-126, doi: 10.1109/UralCon52005.2021.9559526.

[26] M. Vijeh, E. Samadaei, M. Rezanejad, H. Vahedi and K. Al-Haddad, "Design and implementation of a new three source topology of multilevel inverters with reduced number of switches," in *IECON 2016 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 6500-6505.

[27] M. Jayabalan, B. Jeevarathinam, and T. Sandirasegarane, "Reduced switch count pulse width modulated multilevel inverter," *IET Power Electronics*, vol. 10, no. 1, pp. 10-17, Jan. 2017.

[28] M. D. Siddique, Mustafa, A. Sarwar, S. Mekhilef, N. B. M. Shah, M. Seyedamahmousian, A. Stojcevski, B. Horan, and K. Ogura, "Single phase symmetrical and asymmetrical design of multilevel inverter topology with reduced number of switches," in *IEEE 2018 IEEMA Engineer Infinite Conference*, 2018, pp. 1-6.

[29] V. Anand, and V. Singh, "Compact symmetrical and asymmetrical multilevel inverter with reduced switches," *International Transactions on Electrical Energy Systems*, vol. 30, no. 8, pp. 12458, Apr. 2020.

[30] E. Najafi, and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 11, pp. 4148-4154, Nov. 2012.

[31] K. K. Gupta and S. Jain, "A Novel Multilevel Inverter Based on Switched DC Sources," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3269-3278, Jul. 2014.

[32] V. Thiyagarajan, and P. Somasundaram, "Modified seven level symmetric inverter with reduced switch count," *Advances in Natural and Applied Sciences*, vol. 11, no. 7, pp. 264-272, May. 2017.

[33] S. S. Lee, M. Sidorov, N. R. N. Idris and Y. E. Heng, "A Symmetrical Cascaded Compact-Module Multilevel Inverter (CCM-MLI) With Pulse width Modulation," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4631-4639, Jun. 2018.

[34] A. Jafari et al, "Comparison of wide-band-gap technologies for soft-switching losses at high frequencies," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 12595-12600, Dec. 2020.

[35] E. Samadaei, S. A. Gholamian, A. Sheikholeslami and J. Adabi, "An envelope type (e-type) module: asymmetric multilevel inverters with reduced components," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7148-7156, Nov. 2016.

[36] R. S. Alishah, S. H. Hosseini, E. Babaei and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," IEEE Transactions on Industrial Electronics, vol. 64, no. 3, pp. 2072-2080, March 2017.

[37] D. Krishnachaitanya, and A. Chitra, "Quantitative analysis of asymmetric multilevel inverters with reduced device count from reliability and cost function perspective—a review," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11068-11086, Oct. 2021.

[38] B. Wang, J. Cai, X. Du and L. Zhou, "Review of power semiconductor device reliability for power converters," CPSS Transactions on Power Electronics and Applications, vol. 2, no. 2, pp. 101-117, 2017.

[39] V. de Nazareth Ferreira, A. F. Cupertino, H. A. Pereira, A. V. Rocha, S. I. Seleme, and B. de Jesus Cardoso Filho, "Design and selection of high reliability converters for mission critical industrial applications: A rolling mill case study," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4938-4947, Apr. 2016.

[40] M. Handbook, *Electronic Reliability Design (MIL-HDBK-338B).* Washington DC: US Department of Defense, 1998.

[41] O'Connor, Andrew N. *Probability Distributions Used in Reliability Engineering.* United States: Quanterion Solutions Incorporated, 2011.

[42] M. Handbook, *Reliability Prediction of Electronic Equipment (MIL-HDBK-217F).* Washington DC: US Government Printing Office, 1986, Sec.

[43] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590-602, Feb. 2015.

[44] M. Andresen, V. Raveendran, G. Buticchi, and M. Liserre, "Lifetime based power routing in parallel converters for smart transformer application," *IEEE Transactions on Power Electronics*, vol. 65, no. 2, pp. 1675-1684, Feb. 2018.

[45] O'Connor, Andrew N. *Probability Distributions Used in Reliability Engineering.* United States: Quanterion Solutions Incorporated, 2011.

[46] M. Handbook, *Electronic Reliability Design (MIL-HDBK-338B).* Washington DC: US Department of Defense, 1998.

[47] J. P. Kozak *et al*., "Stability, Reliability, and Robustness of GaN Power Devices: A Review," in *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 8442-8471, July 2023, doi: 10.1109/TPEL.2023.3266365.